FIG.1

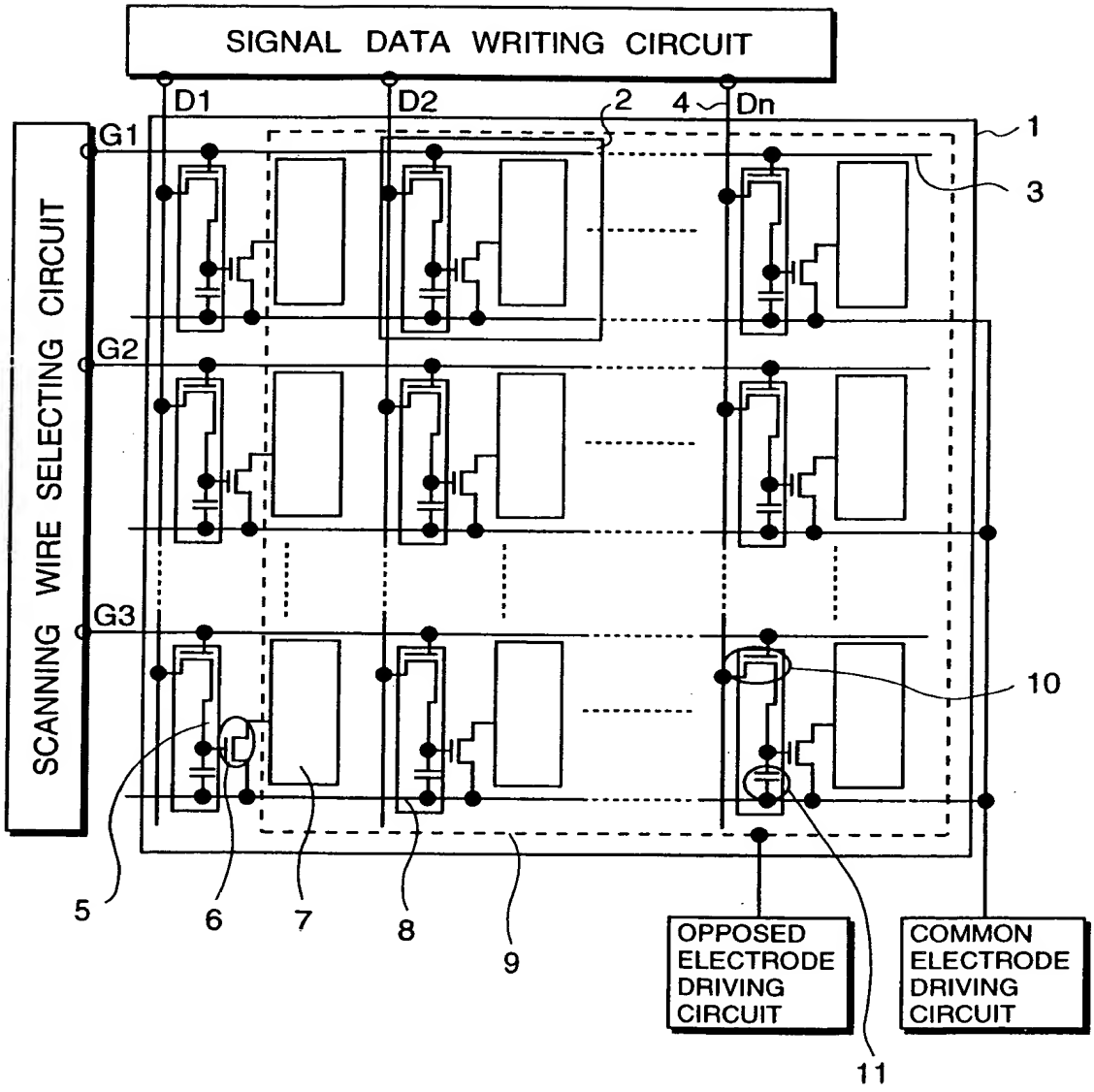

SIGNAL DATA WRITING CIRCUIT
D1
D2
2
4
Dn
1
3
G1
G2
G3
SCANNING WIRE SELECTING CIRCUIT
10
5
6
7
8
9
11
OPPOSED ELECTRODE DRIVING CIRCUIT
COMMON ELECTRODE DRIVING CIRCUIT

FIG.2

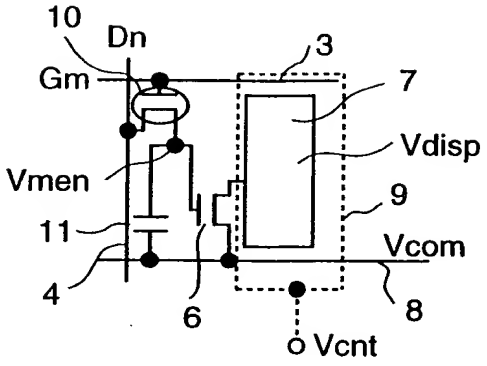

10
Dn
3
Gm
7
Vdisp
Vmen
9
11
Vcom
4
6
8
Vcnt

FIG.3

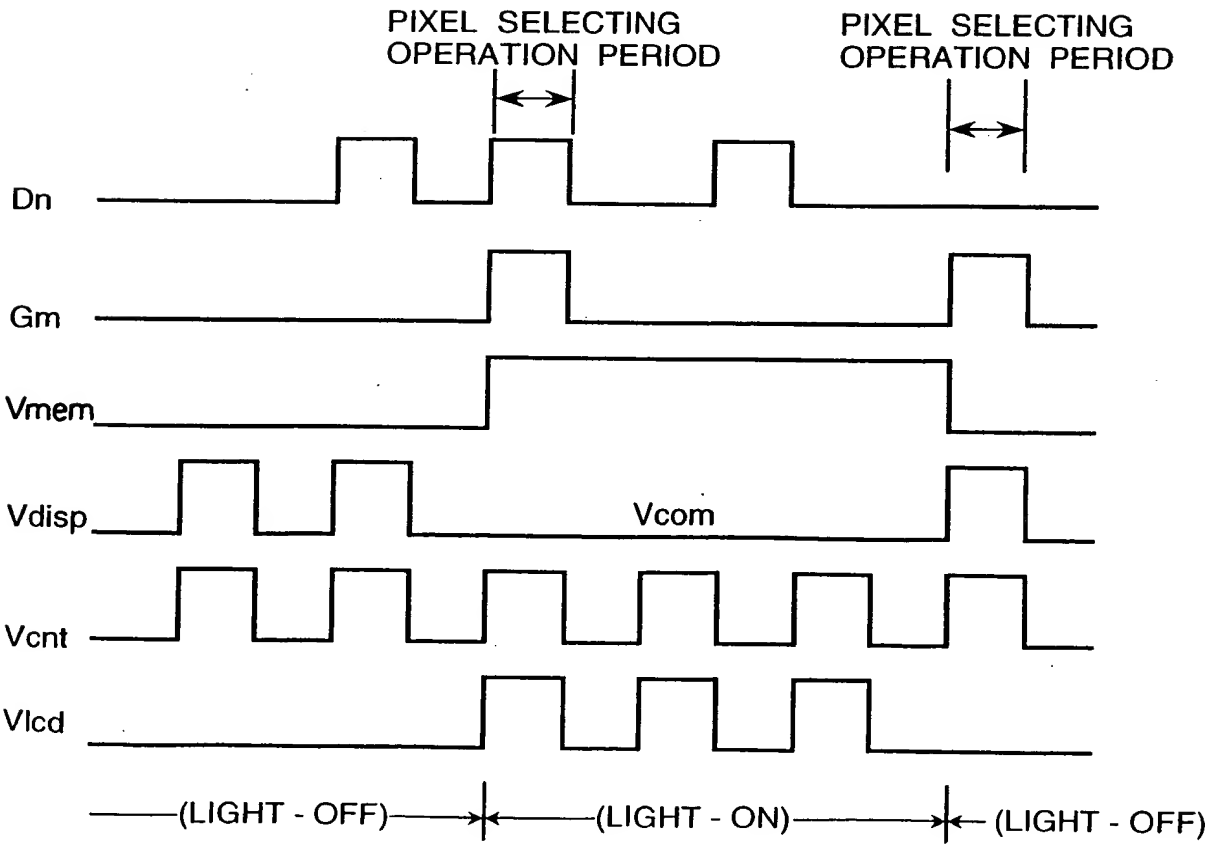

PIXEL SELECTING OPERATION PERIOD
PIXEL SELECTING OPERATION PERIOD
Dn
Gm
Vmem
Vdisp
Vcom
Vcnt
Vlcd
(LIGHT - OFF)
(LIGHT - ON)
(LIGHT - OFF)

FIG.4

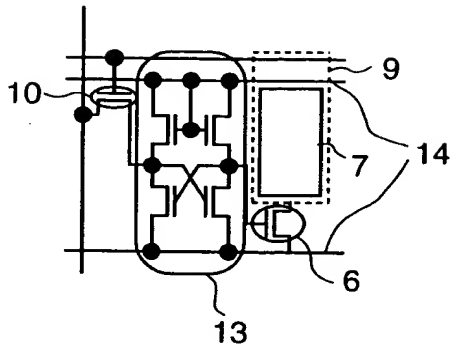


FIG.5

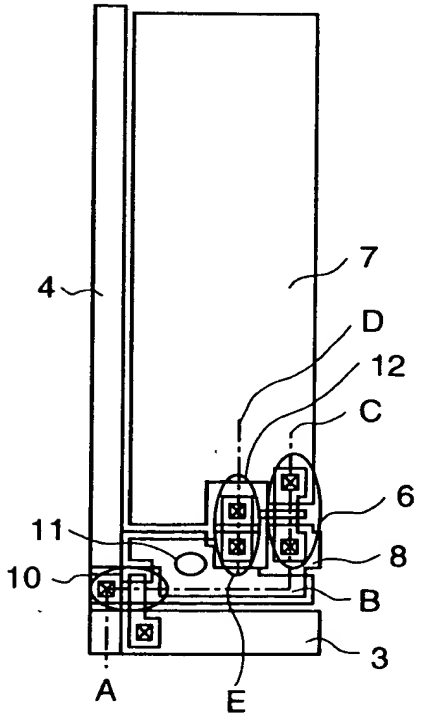


FIG.6

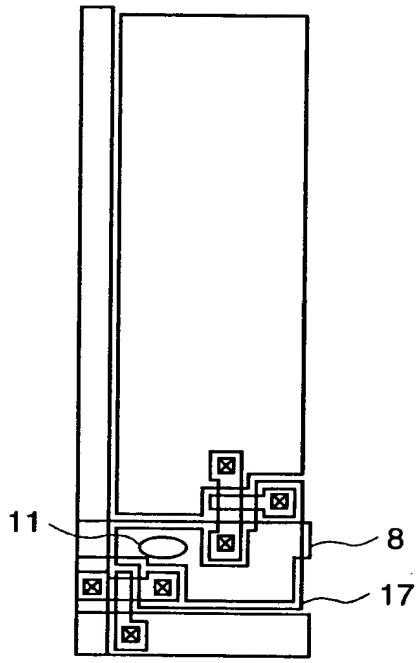


FIG.7

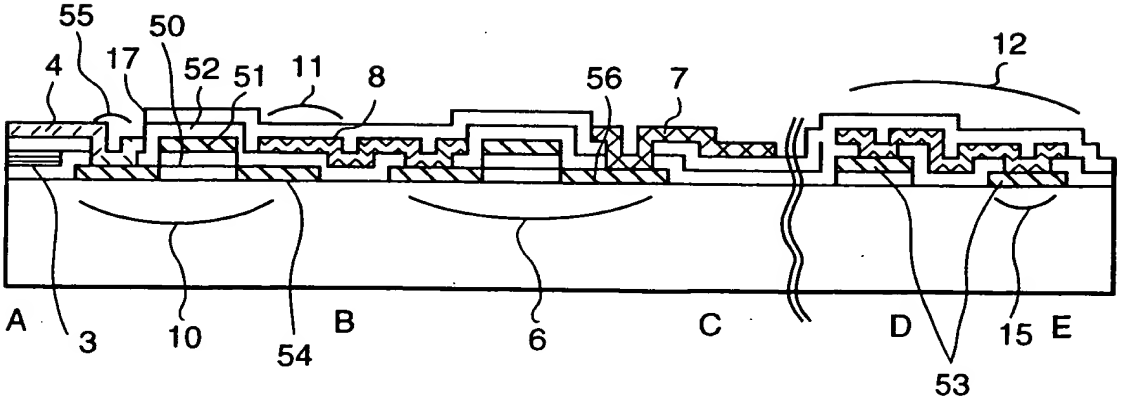


FIG.8

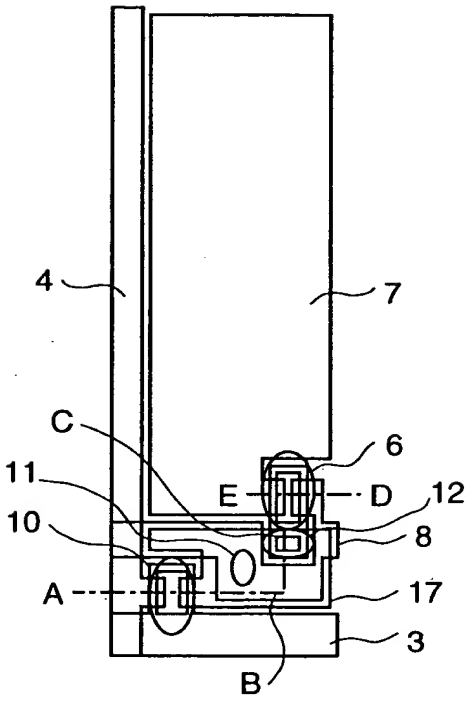


FIG.9

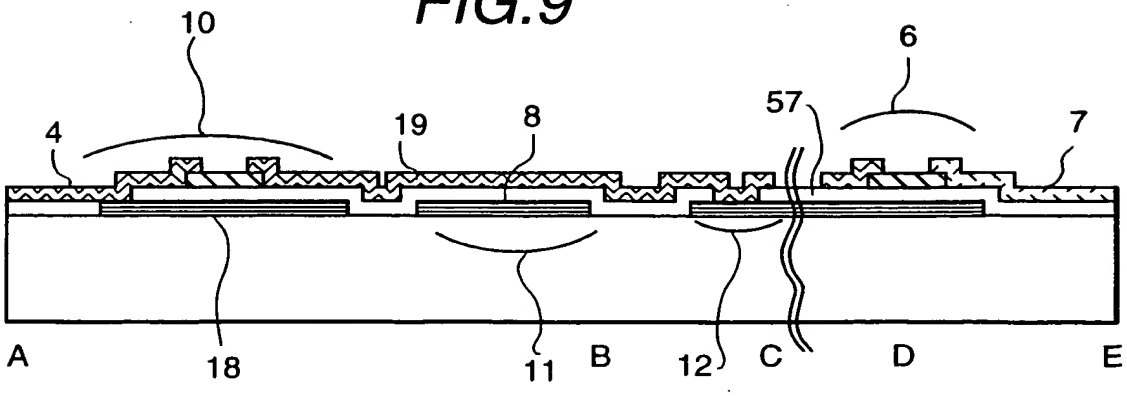


FIG. 10

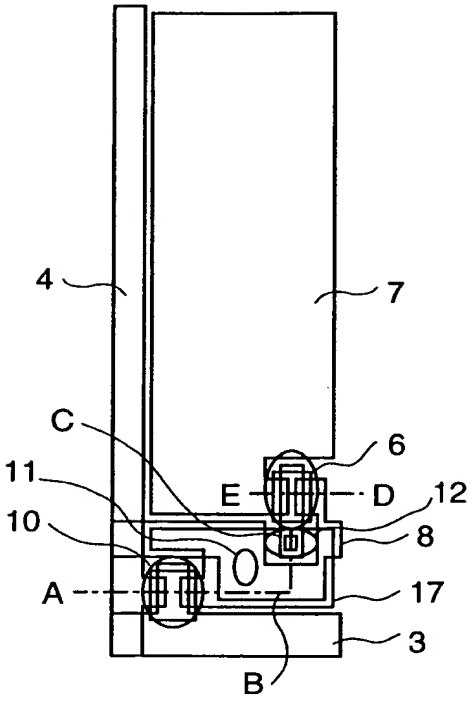


FIG. 11

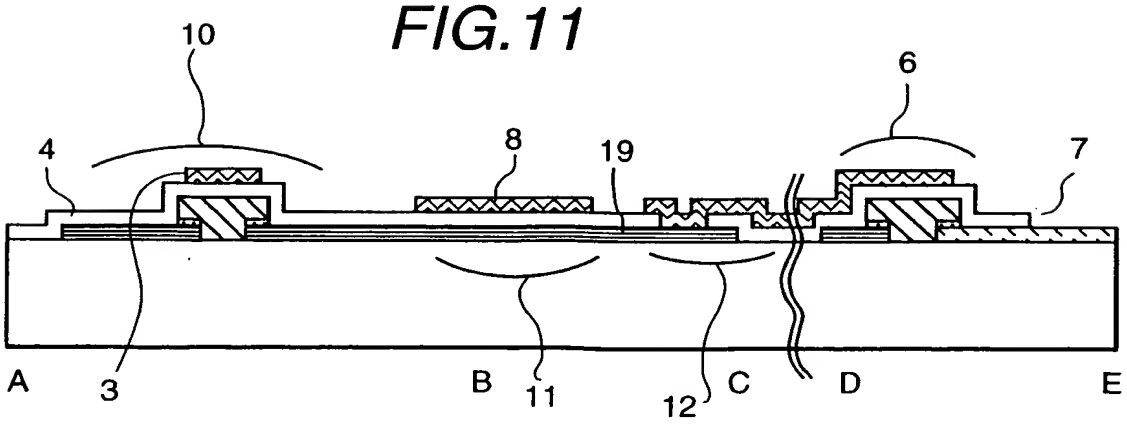


FIG. 12

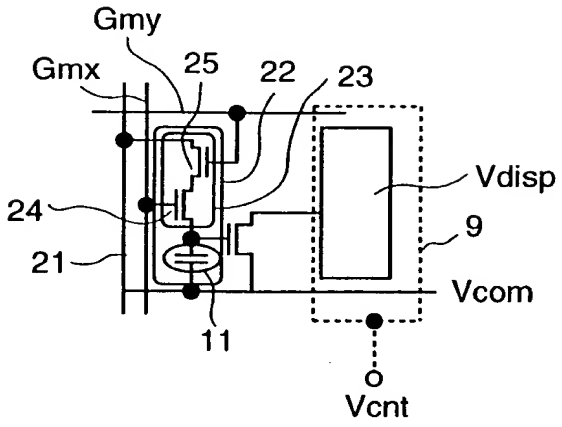

Gmy
Gmx
25
22
23
Vdisp
24
9
21
Vcom
11
Vcnt

FIG. 13

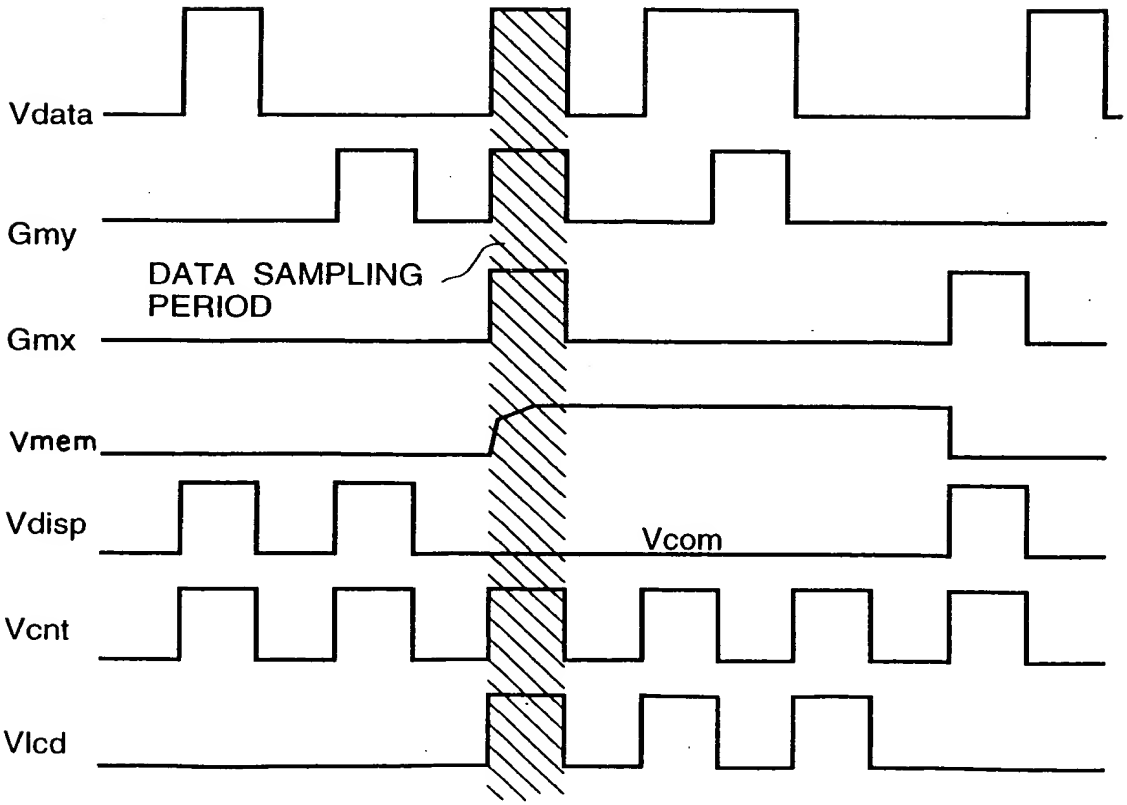

Vdata
Gmy
DATA SAMPLING PERIOD
Gmx
Vmem
Vdisp
Vcom
Vcnt
Vlcd

FIG. 14

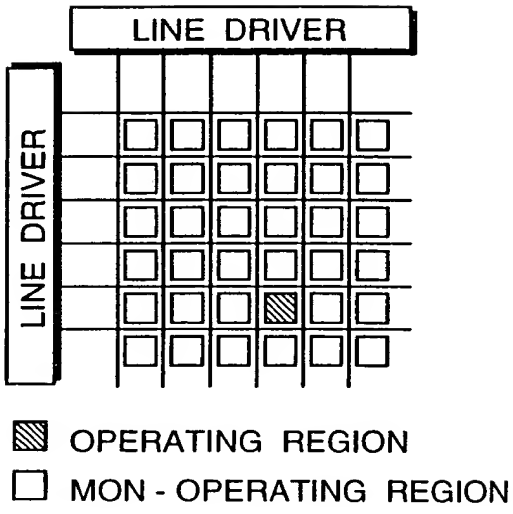

LINE DRIVER
LINE DRIVER
OPERATING REGION
MON - OPERATING REGION

FIG. 15

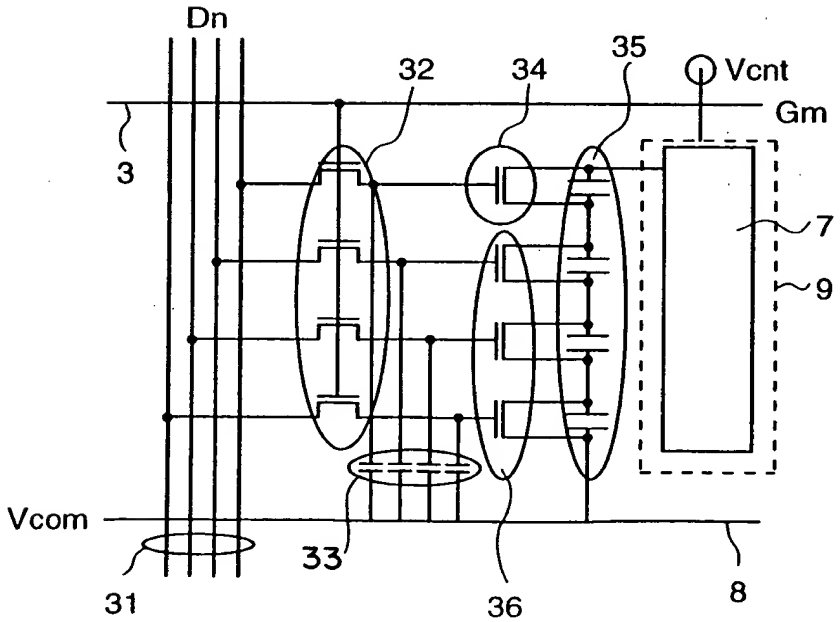

Dn
32
34
35
Vcnt
Gm
3
7
9
Vcom
33
31
36
8

FIG.16

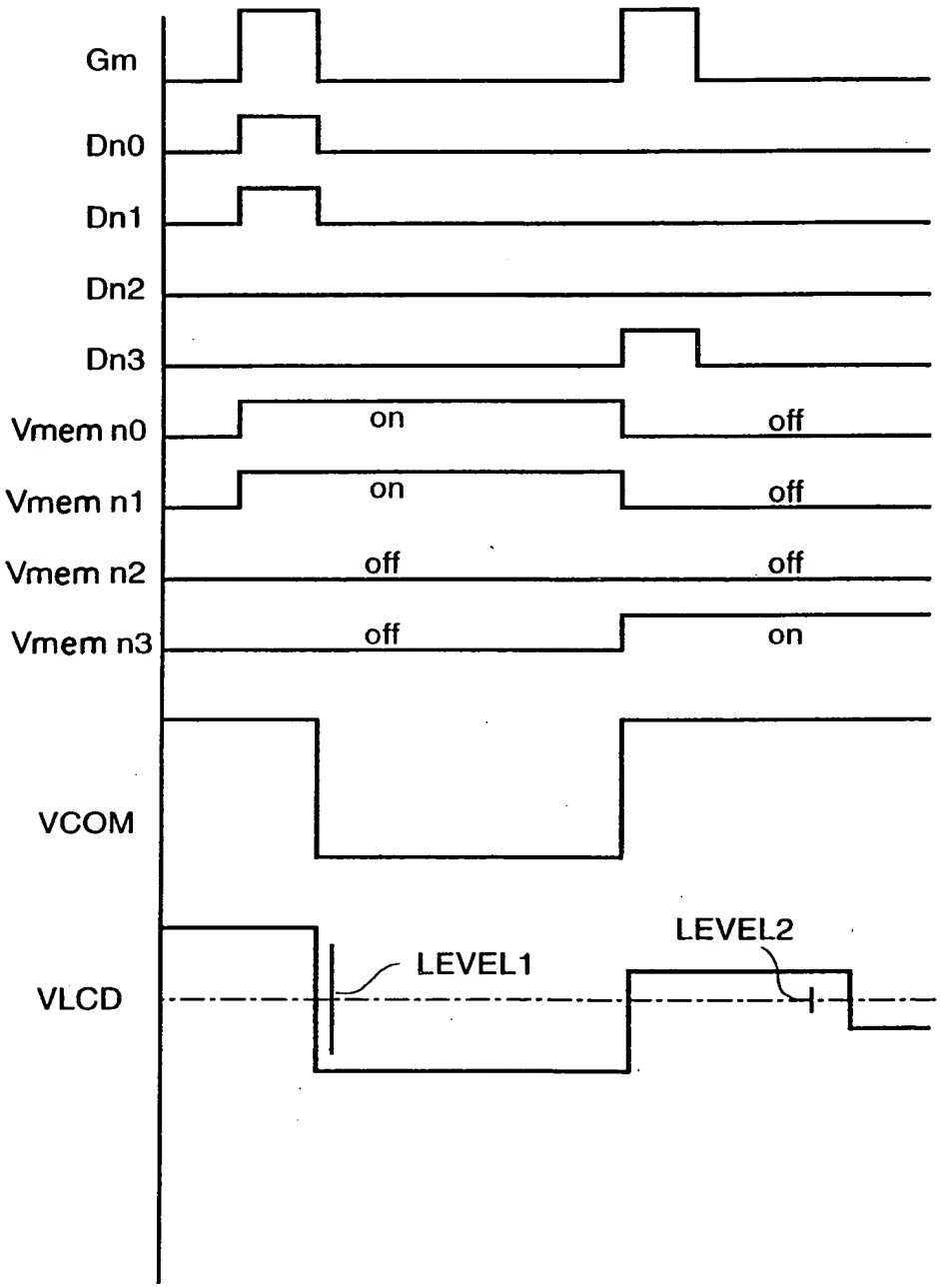

Gm
Dn0
Dn1
Dn2
Dn3
Vmem n0
on
off
Vmem n1
on
off
Vmem n2
off
off
Vmem n3
off
on
VCOM
VLCD
LEVEL1
LEVEL2

FIG. 17

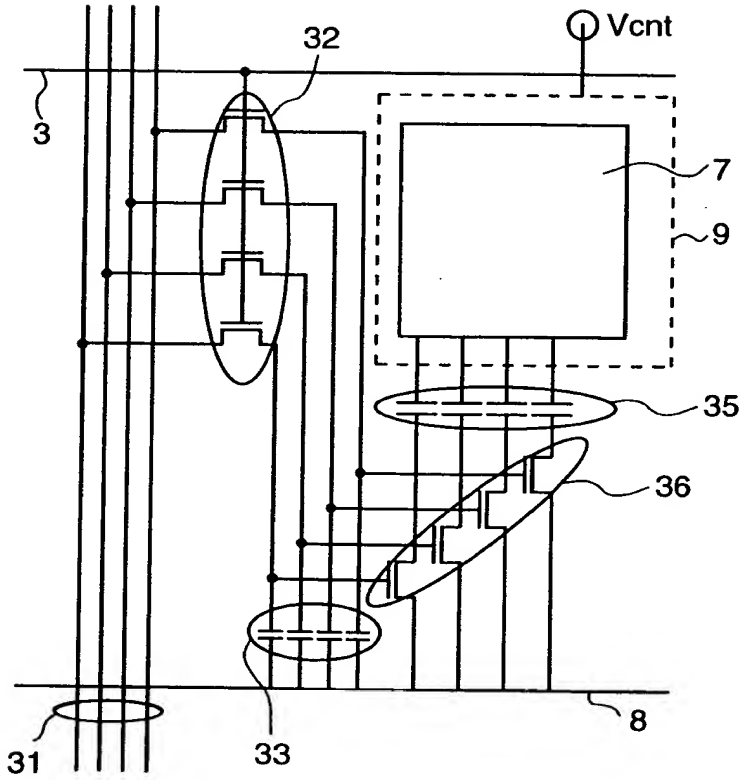


FIG. 18

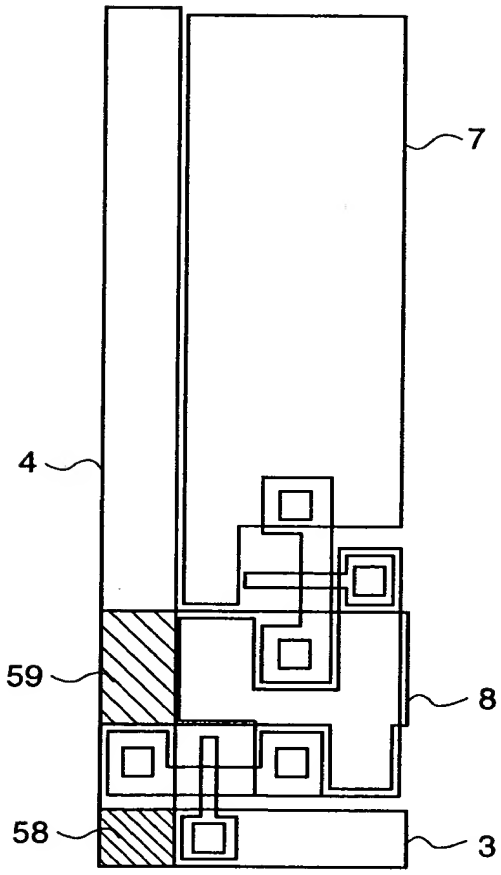


FIG. 19
(PRIOR ART)

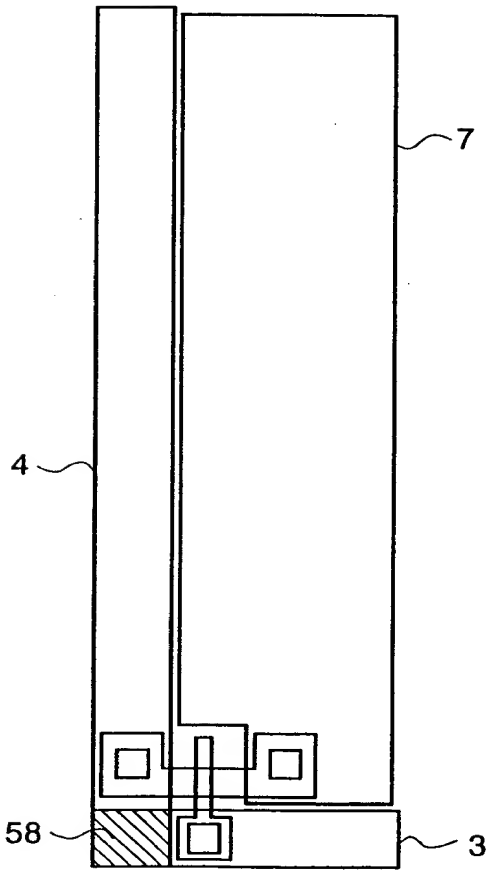


FIG.20

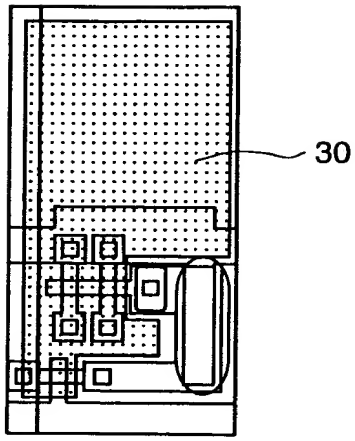


FIG.21

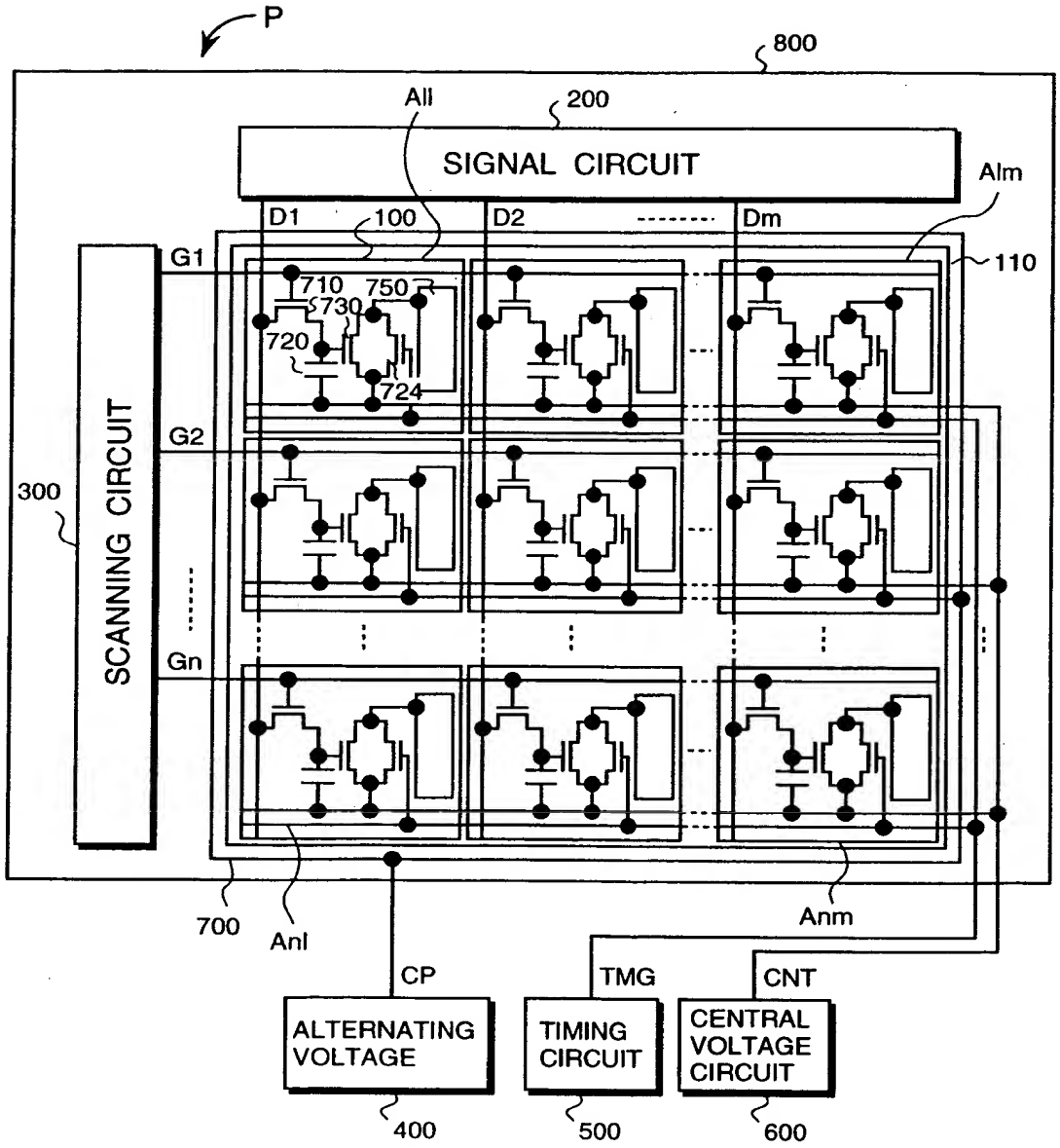

P
800
All
200
SIGNAL CIRCUIT
Alm
D1
100
D2
Dm
110
G1
710
750
730
720
724
G2
300
SCANNING CIRCUIT
Gn
700
Anl
Anm
CP
TMG
CNT
ALTERNATING VOLTAGE
TIMING CIRCUIT
CENTRAL VOLTAGE CIRCUIT
400
500
600

FIG.22

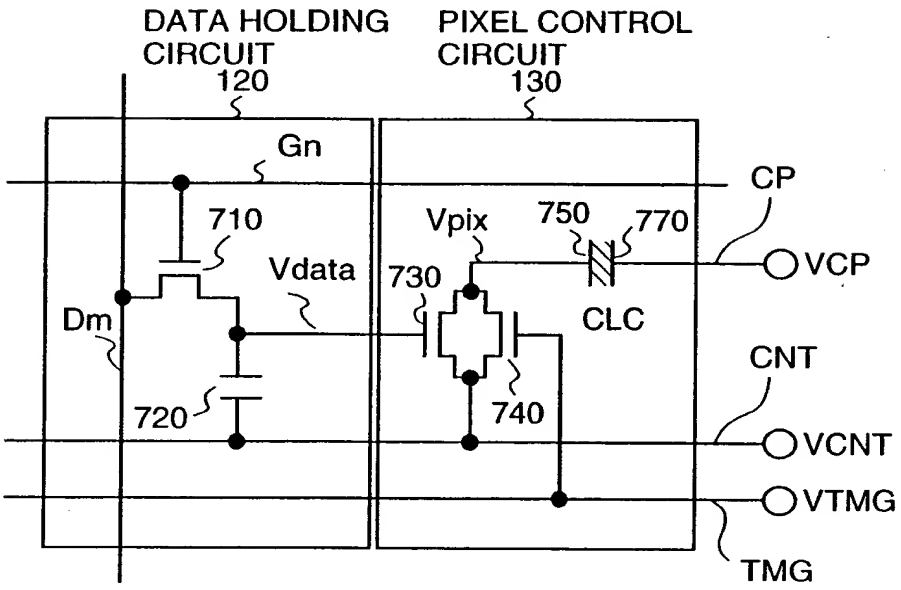

DATA HOLDING CIRCUIT
120
PIXEL CONTROL CIRCUIT
130
Gn
710
Vdata
Dm
720
Vpix
750
770
730
740
CLC
CP
VCP
CNT
VCNT
VTMG
TMG

FIG.23

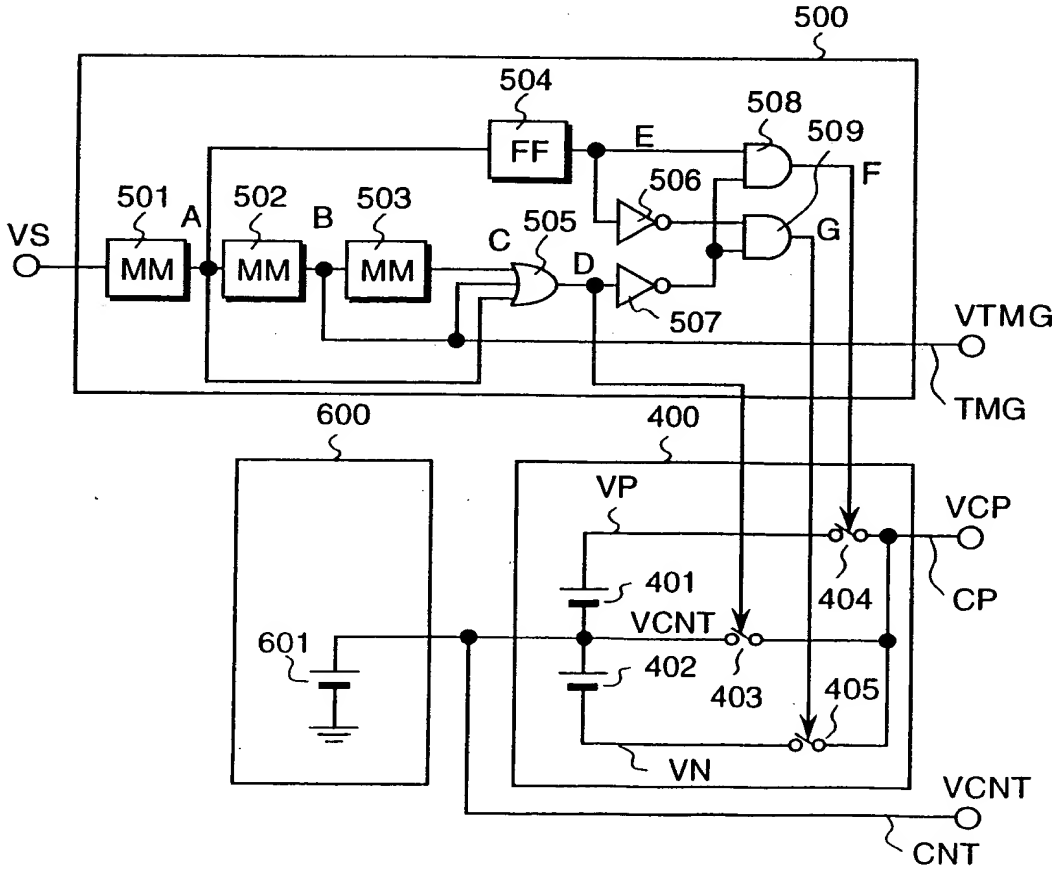

500
504
FF
508
509
E
F
506
501
A
502
B
503
VS
MM
MM
MM
C
505
D
G
507
VTMG
TMG
600
400
VP
VCP
401
404
CP
VCNT
601
402
403
405
VN
VCNT
CNT

FIG.24

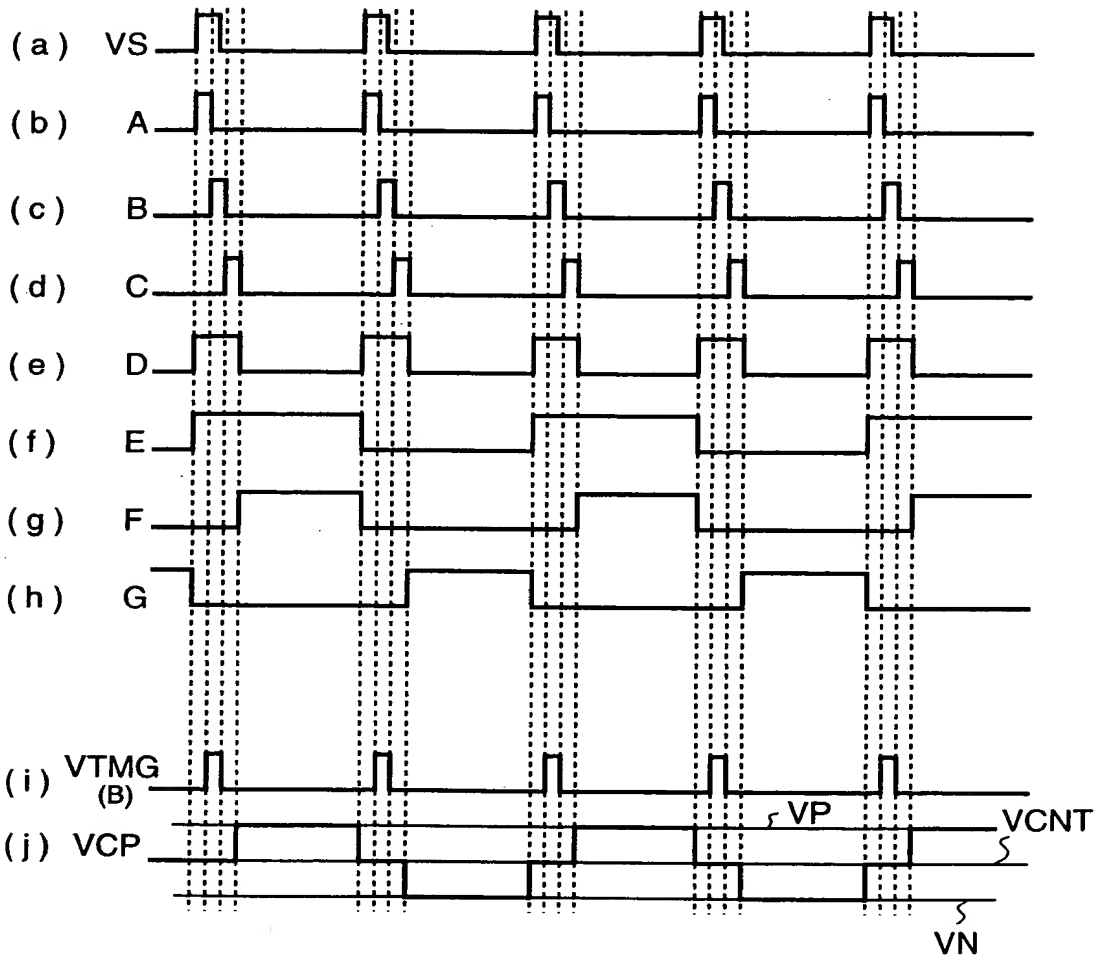


FIG.25

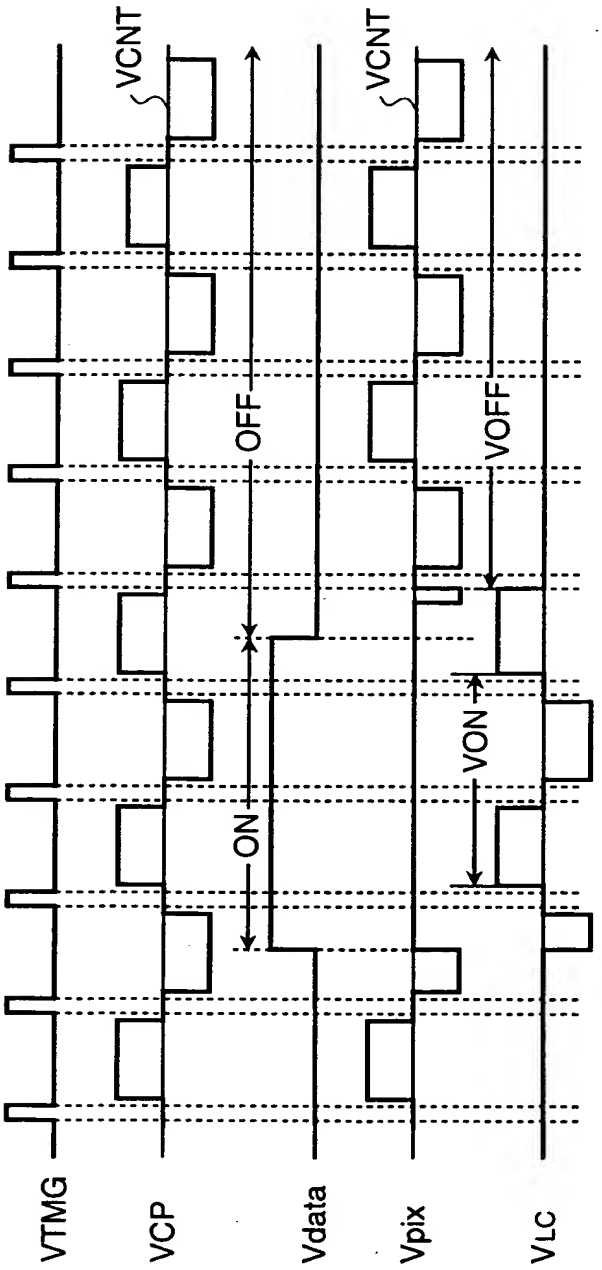


FIG.26

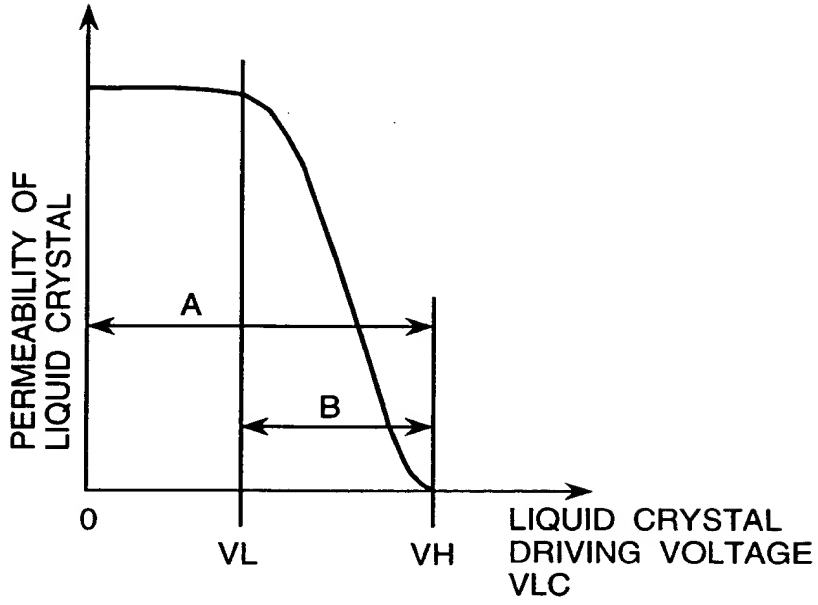

PERMEABILITY OF LIQUID CRYSTAL
A
B
0
VL
VH
LIQUID CRYSTAL DRIVING VOLTAGE VLC

FIG.28

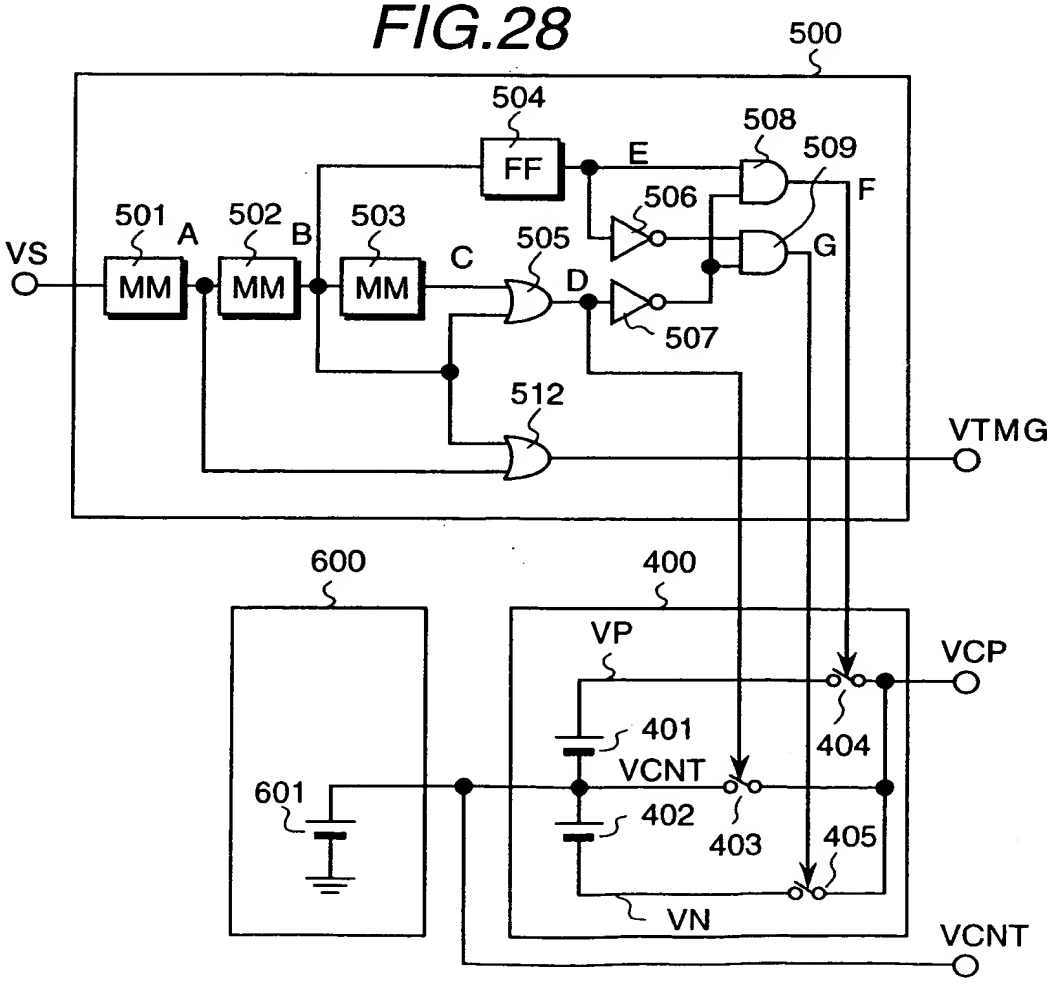

500
504
FF
E
508
509
F
506
501
A
502
B
503
C
505
D
G
VS
MM
MM
MM
507
512
VTMG
600
400
VP
VCP
401
404
VCNT
601
402
403
405
VN
VCNT

FIG.27

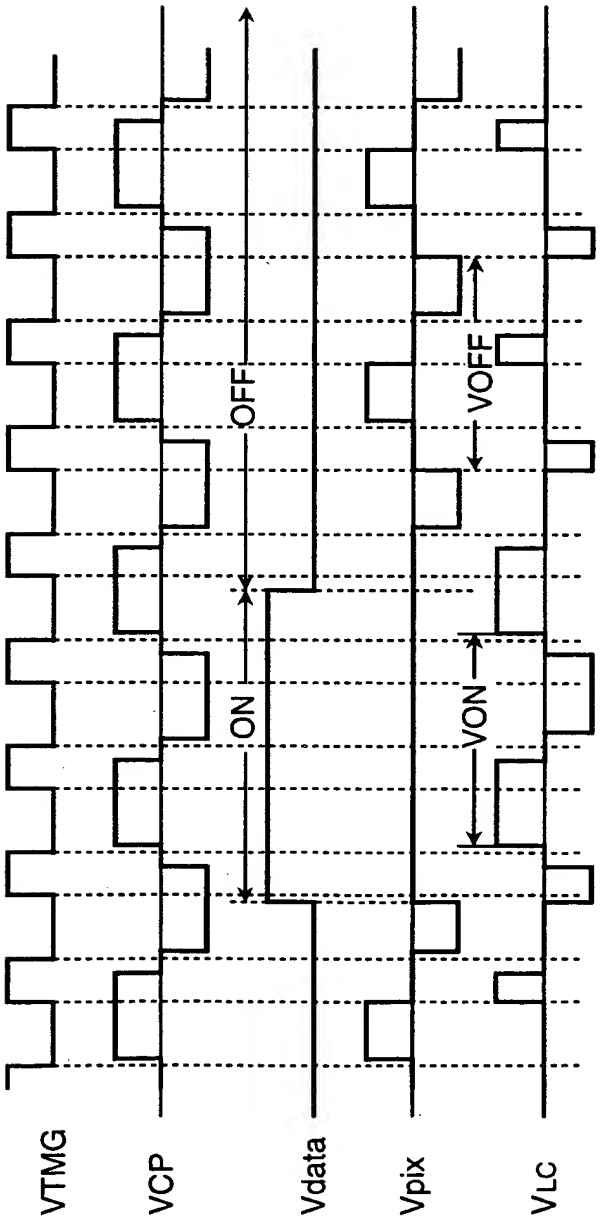


FIG.29

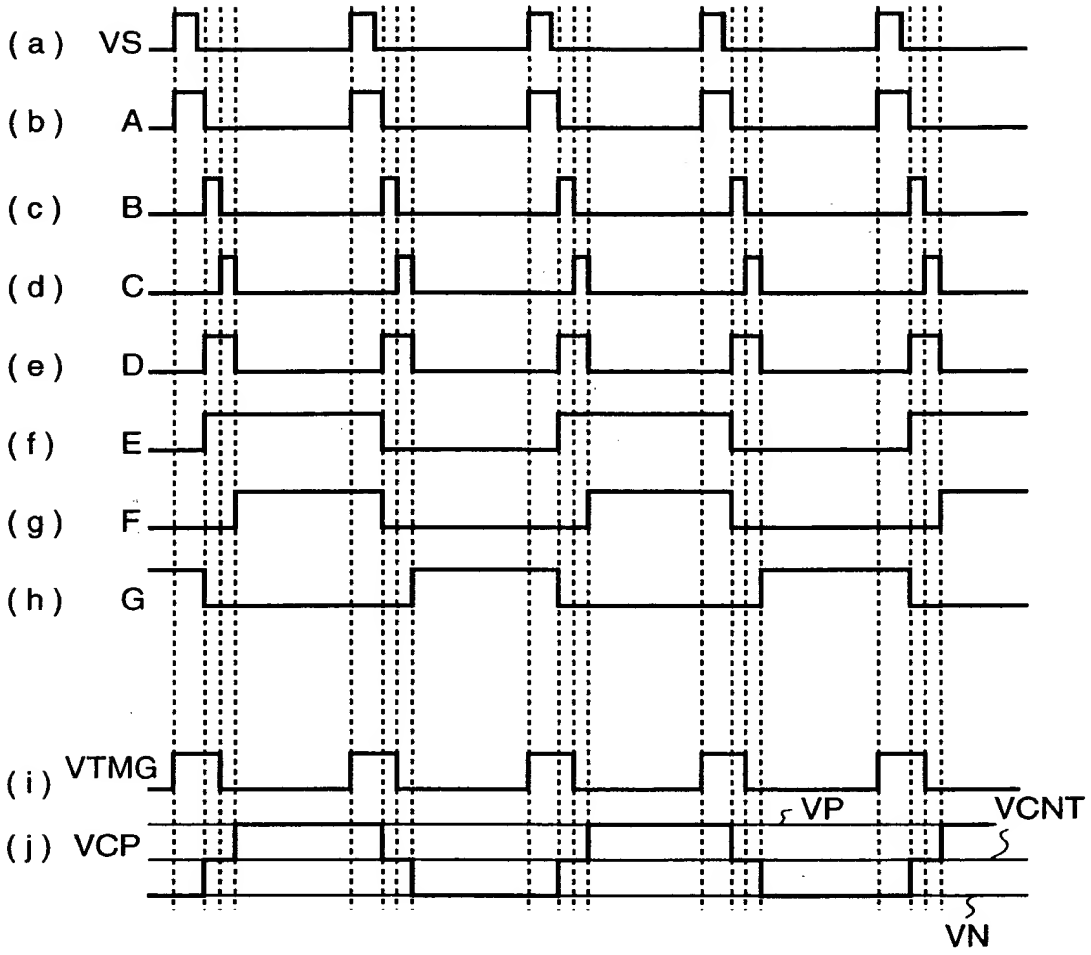

(a) VS
(b) A
(c) B
(d) C
(e) D
(f) E
(g) F
(h) G
(i) VTMG
(j) VCP
VP
VCNT
VN

FIG.30

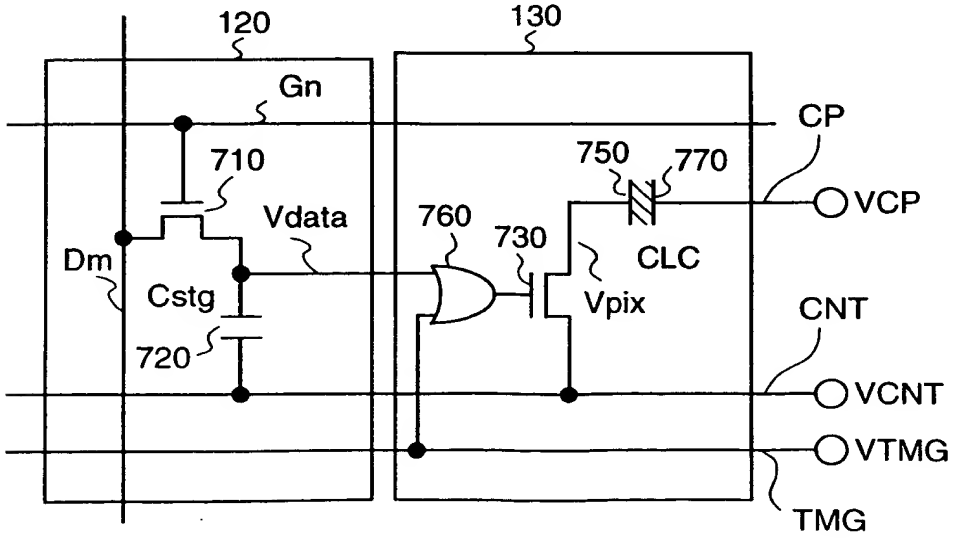

120
130
Gn
710
Vdata
Dm
Cstg
720
760
730
750
770
CLC
Vpix
CP
VCP
CNT
VCNT
VTMG
TMG

FIG.31

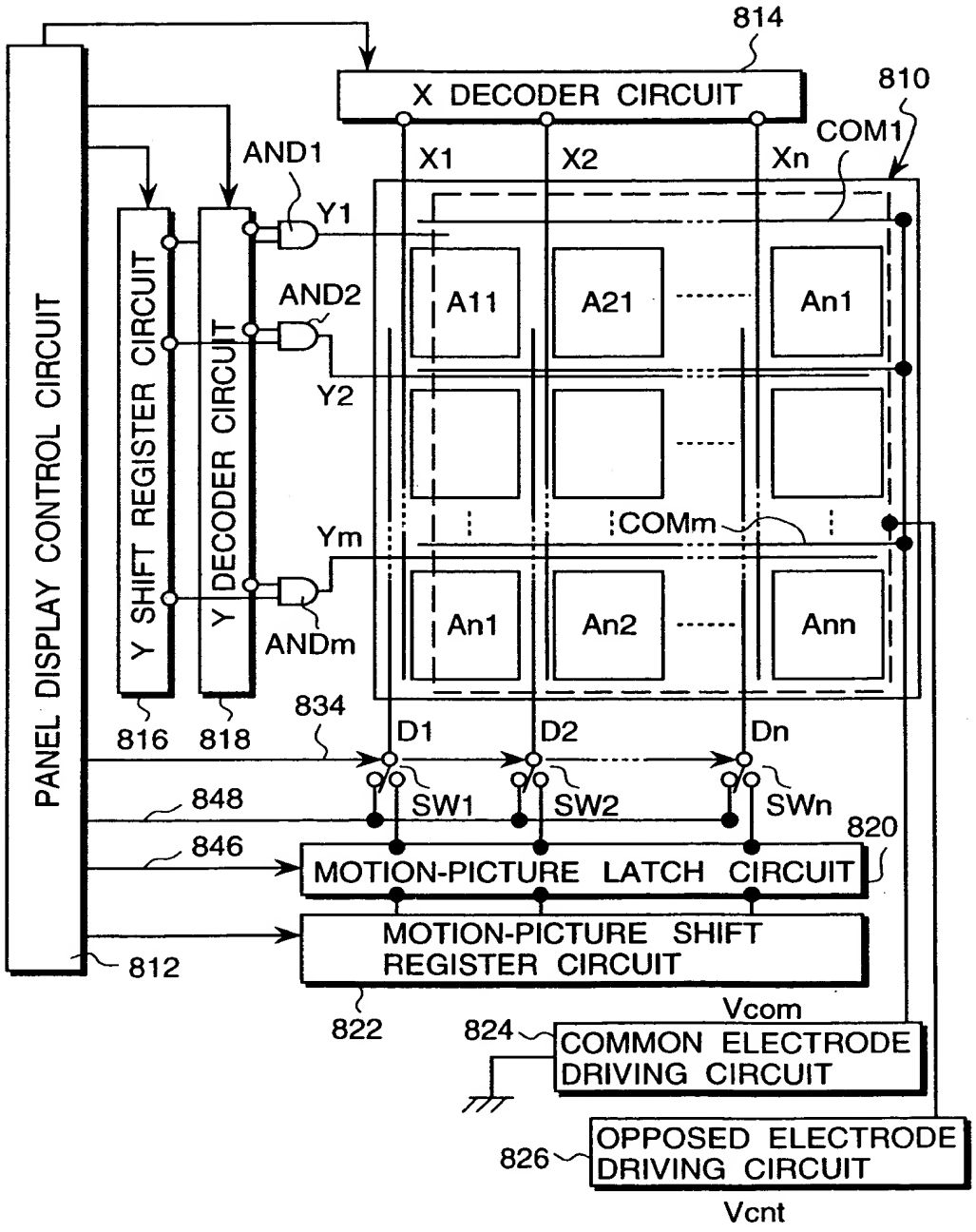

814
X DECODER CIRCUIT
810
COM1
AND1
X1
X2
Xn
Y1
AND2
A11
A21
An1
Y2
Ym
COMm
An1
An2
Ann
ANDm
PANEL DISPLAY CONTROL CIRCUIT
Y SHIFT REGISTER CIRCUIT
Y DECODER CIRCUIT
816
818
834
D1
D2
Dn
848
SW1
SW2
SWn
820
846
MOTION-PICTURE LATCH CIRCUIT
MOTION-PICTURE SHIFT REGISTER CIRCUIT
812
822
Vcom
824
COMMON ELECTRODE DRIVING CIRCUIT
826
OPPOSED ELECTRODE DRIVING CIRCUIT
Vcnt

FIG.32

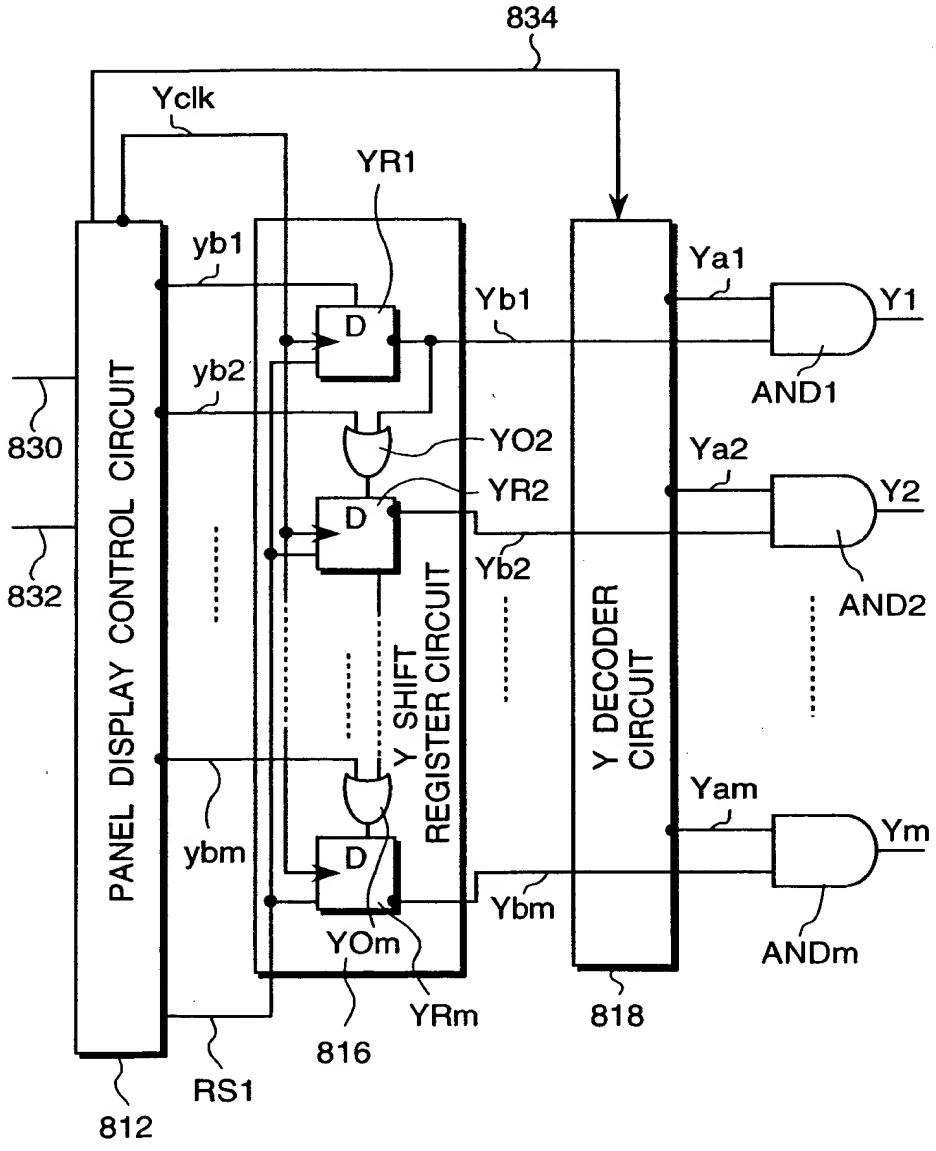

834
Yclk
YR1
yb1
yb2
830
832
PANEL DISPLAY CONTROL CIRCUIT
ybm
812
RS1
D
YO2
YR2
Y SHIFT REGISTER CIRCUIT
YOm
YRm
816
Yb1
Yb2
Ybm
Y DECODER CIRCUIT
818
Ya1
Ya2
Yam
Y1
Y2
Ym
AND1
AND2
ANDm

FIG.33

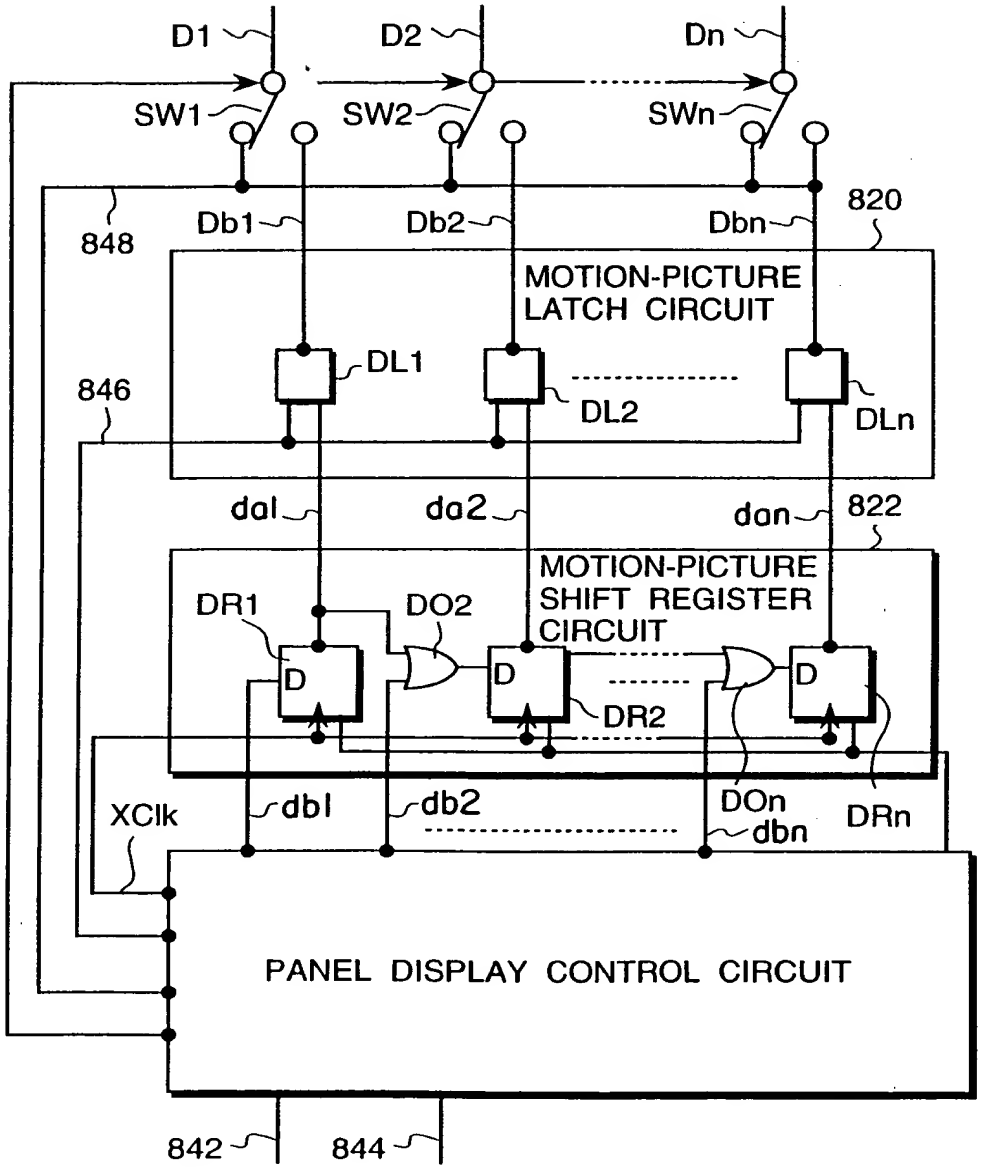

D1
D2
Dn
SW1
SW2
SWn
848
Db1
Db2
Dbn
820
MOTION-PICTURE
LATCH CIRCUIT
DL1
DL2
DLn
846
dal
da2
dan
822
MOTION-PICTURE
SHIFT REGISTER
CIRCUIT
DR1
DO2
D
DR2
XClk
dbl
db2
DOn
dbn
DRn
PANEL DISPLAY CONTROL CIRCUIT
842
844

FIG.34

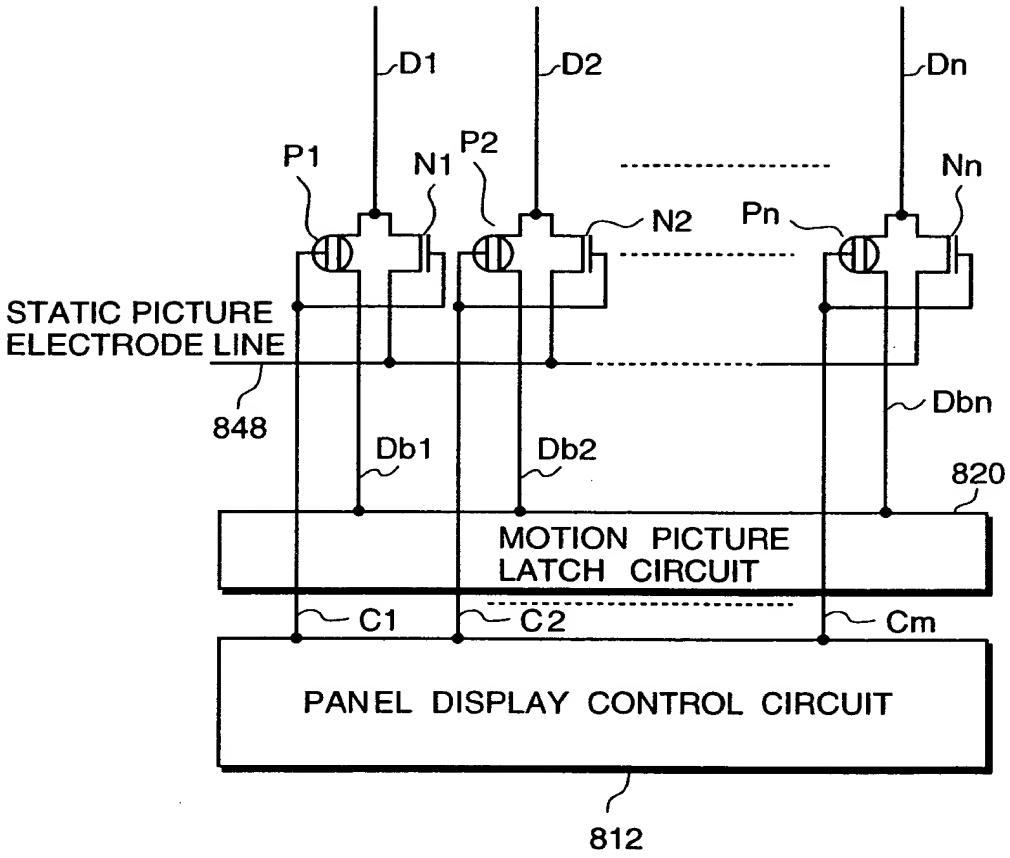

D1
D2
Dn
P1
N1
P2
N2
Pn
Nn
STATIC PICTURE
ELECTRODE LINE
848
Dbn
Db1
Db2
820
MOTION PICTURE
LATCH CIRCUIT
C1
C2
Cm
PANEL DISPLAY CONTROL CIRCUIT
812

FIG.35

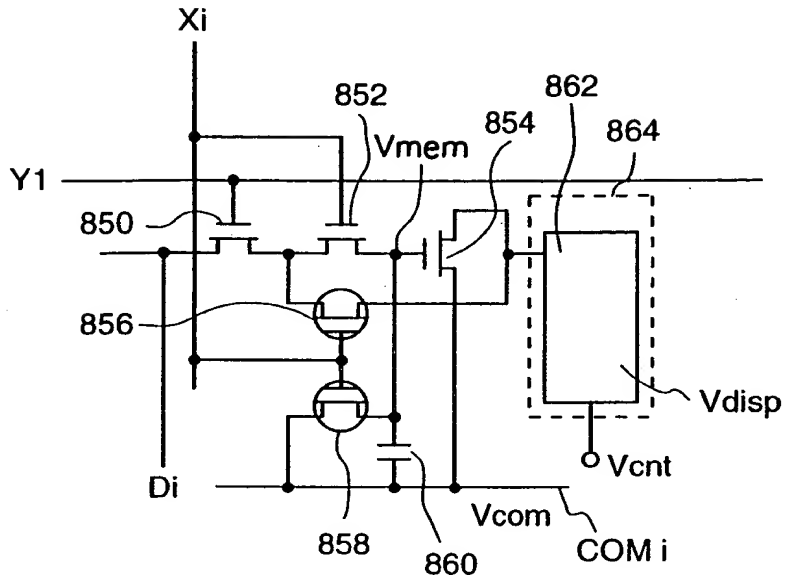

Xi
852
862
854
Vmem
864
Y1
850
856
Vdisp
Vcnt
Di
Vcom
COM i
858
860

FIG.36

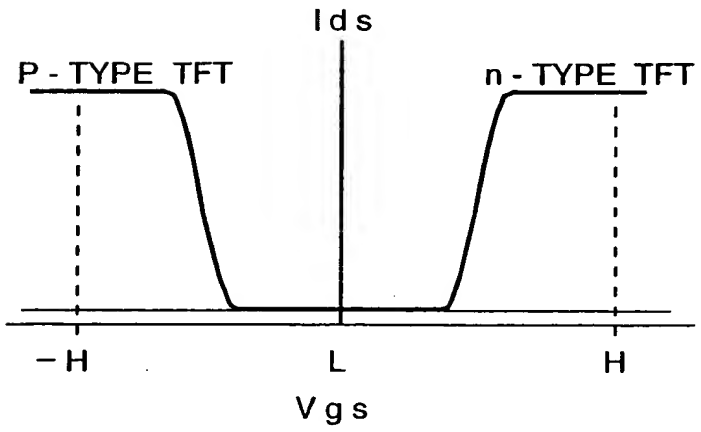

I d s
P - TYPE TFT
n - TYPE TFT
– H
L
H
V g s

FIG.37

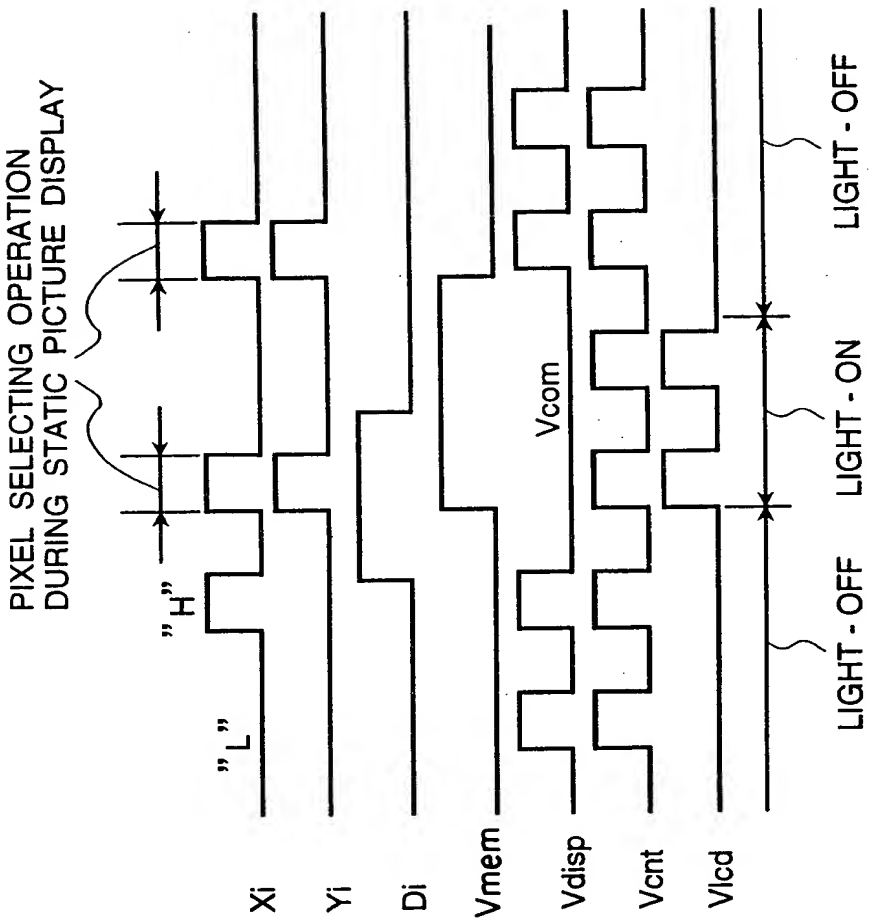

PIXEL SELECTING OPERATION
DURING STATIC PICTURE DISPLAY
"H"
"L"
Xi
Yi
Di
Vmem
Vcom
Vdisp
Vcnt
Vlcd
LIGHT - OFF
LIGHT - ON
LIGHT - OFF

FIG.38

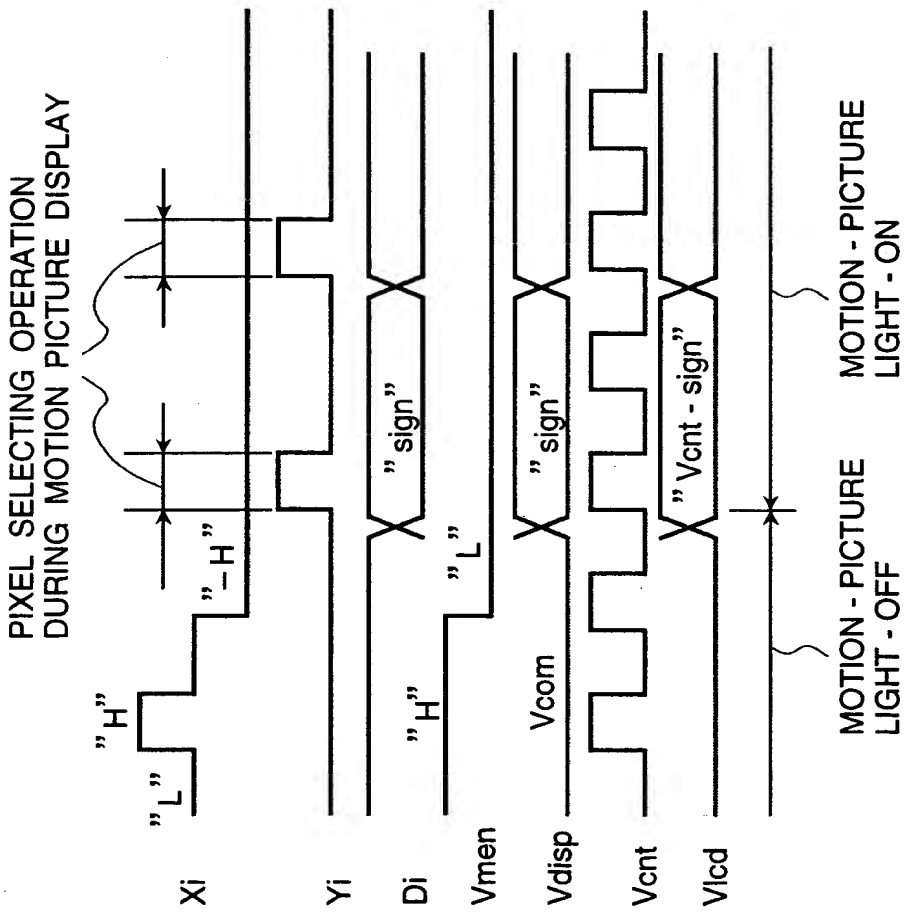

PIXEL SELECTING OPERATION
DURING MOTION PICTURE DISPLAY
"H"
"L"
"-H"
Xi
Yi
Di
"H"
"sign"
Vmen
"L"
Vdisp
Vcom
"sign"
Vcnt
"Vcnt - sign"
Vlcd
MOTION - PICTURE
LIGHT - OFF
MOTION - PICTURE
LIGHT - ON

FIG.39

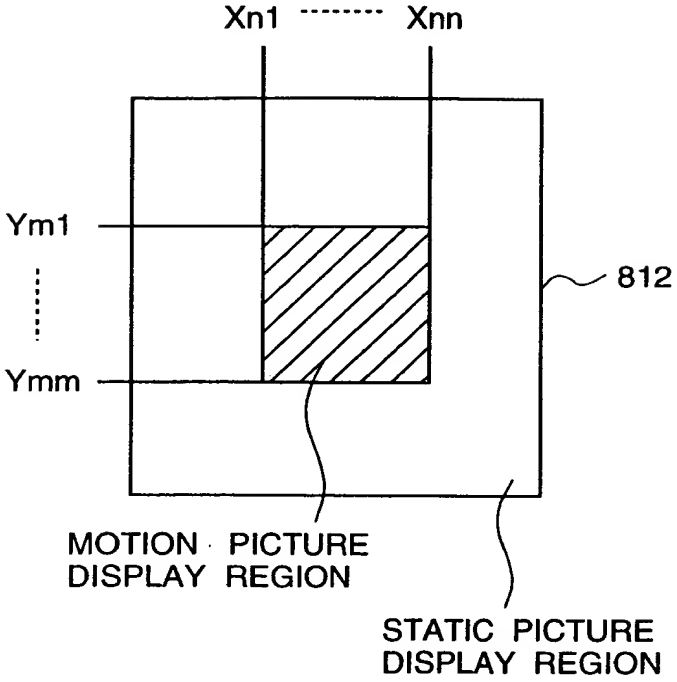

Xn1
Xnn
Ym1
Ymm
812
MOTION PICTURE DISPLAY REGION
STATIC PICTURE DISPLAY REGION

FIG.40

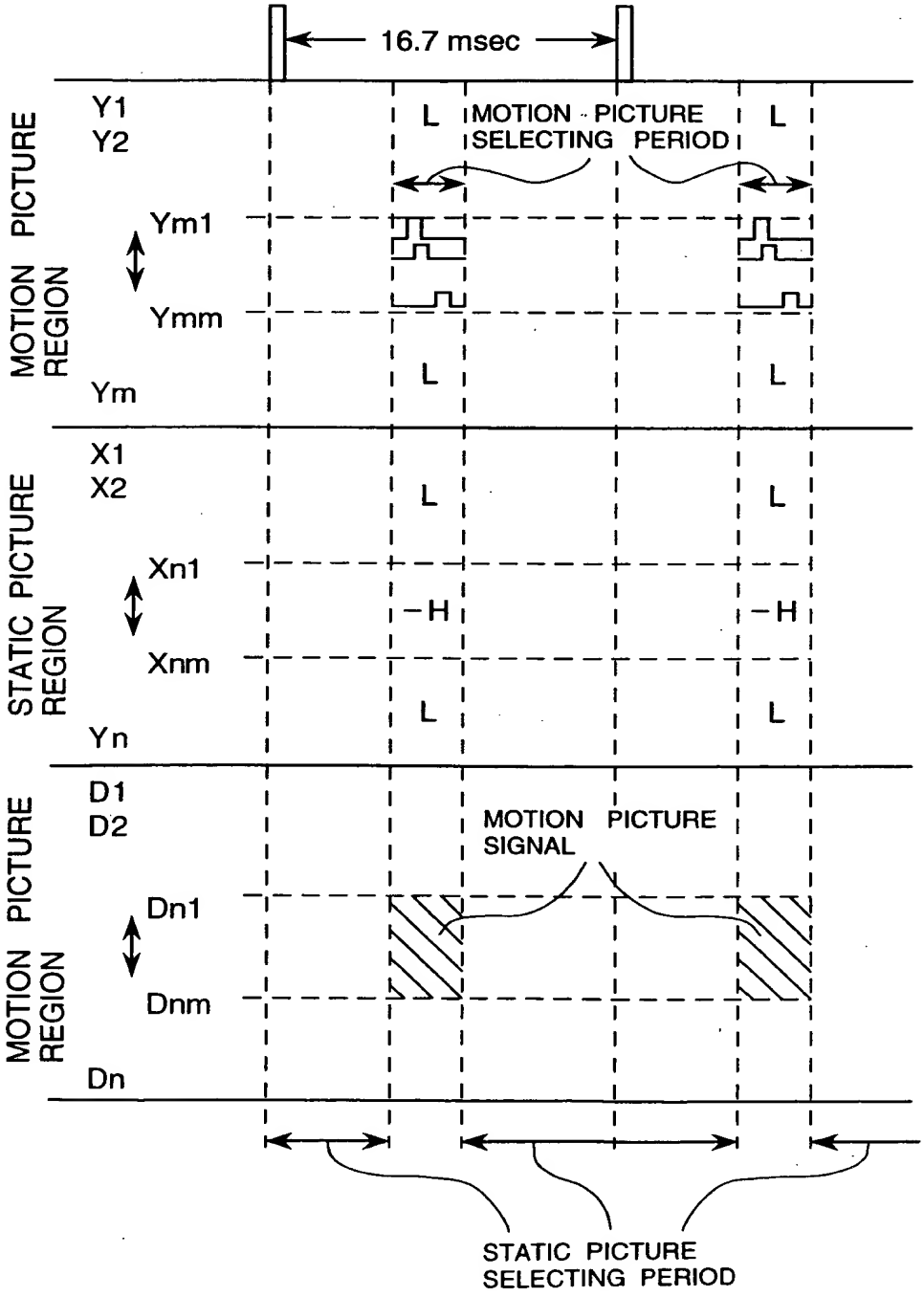

16.7 msec
MOTION PICTURE REGION
Y1
Y2
Ym1
Ymm
Ym
L
MOTION PICTURE SELECTING PERIOD
L
L
L
STATIC PICTURE REGION
X1
X2
Xn1
Xnm
Yn
L
L
H
H
L
L
MOTION PICTURE REGION
D1
D2
Dn1
Dnm
Dn
MOTION PICTURE SIGNAL
STATIC PICTURE SELECTING PERIOD

FIG.41

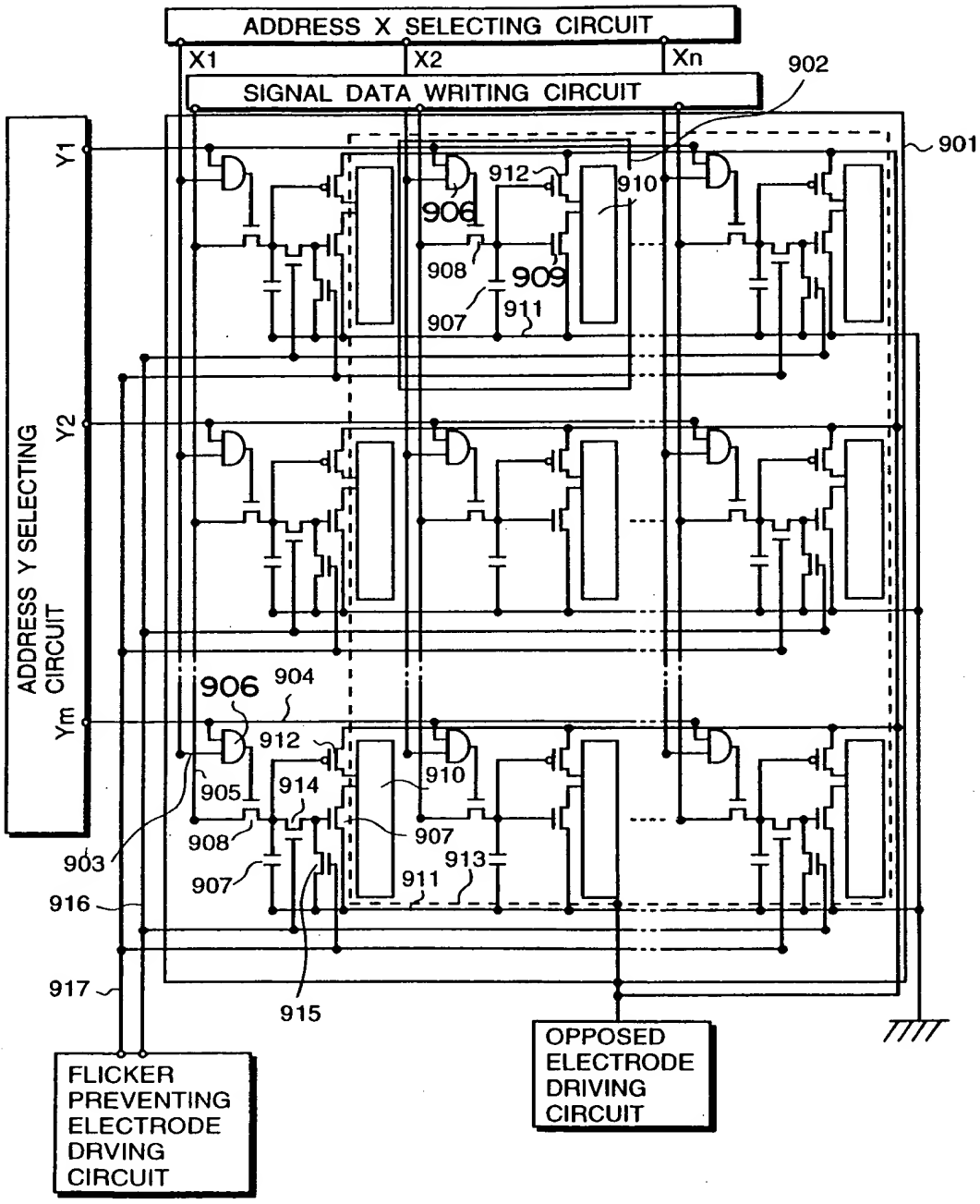

ADDRESS X SELECTING CIRCUIT
X1
X2
Xn
SIGNAL DATA WRITING CIRCUIT
902
901
ADDRESS Y SELECTING CIRCUIT
Y1
Y2
Ym
906
912
910
908
909
907
911
904
905
914
903
913
916
917
915
FLICKER PREVENTING ELECTRODE DRVING CIRCUIT
OPPOSED ELECTRODE DRIVING CIRCUIT

FIG.42

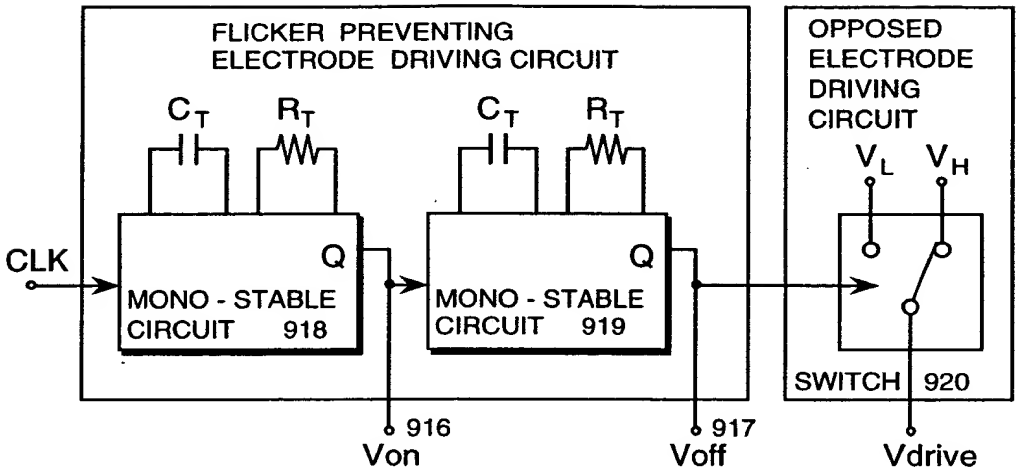

FLICKER PREVENTING
ELECTRODE DRIVING CIRCUIT
C_T
R_T
C_T
R_T
CLK
Q
MONO - STABLE
CIRCUIT 918
Q
MONO - STABLE
CIRCUIT 919
OPPOSED
ELECTRODE
DRIVING
CIRCUIT
V_L
V_H
SWITCH 920
916
Von
917
Voff
Vdrive

FIG.43

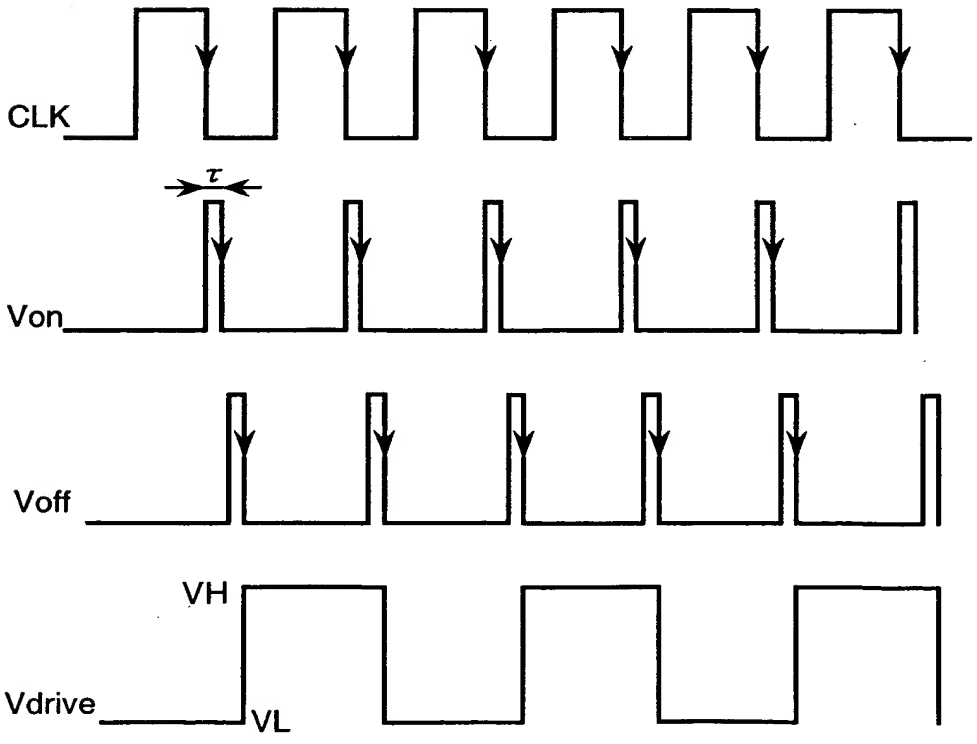

CLK
τ
Von
Voff
VH
Vdrive
VL

FIG.44A

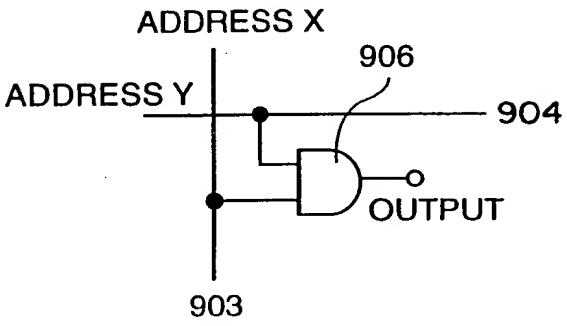


FIG.44B

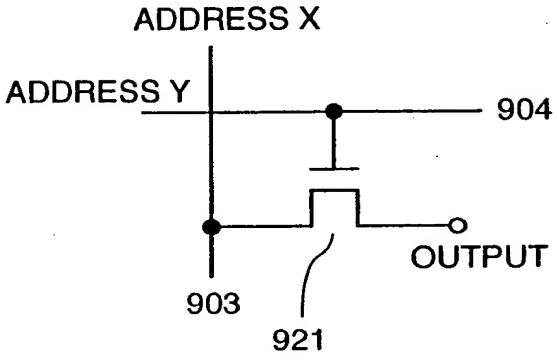


FIG.45

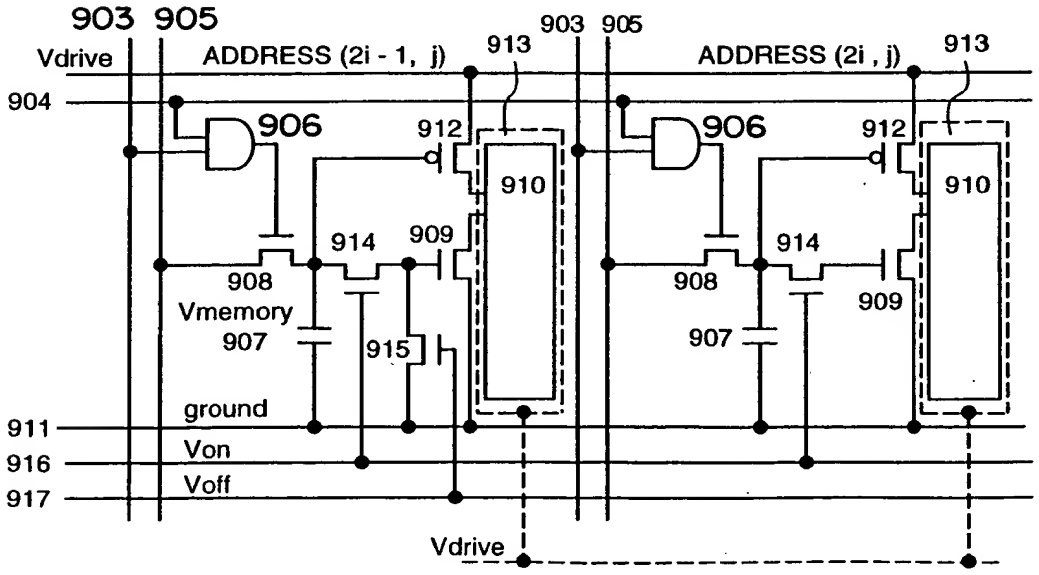


FIG.46

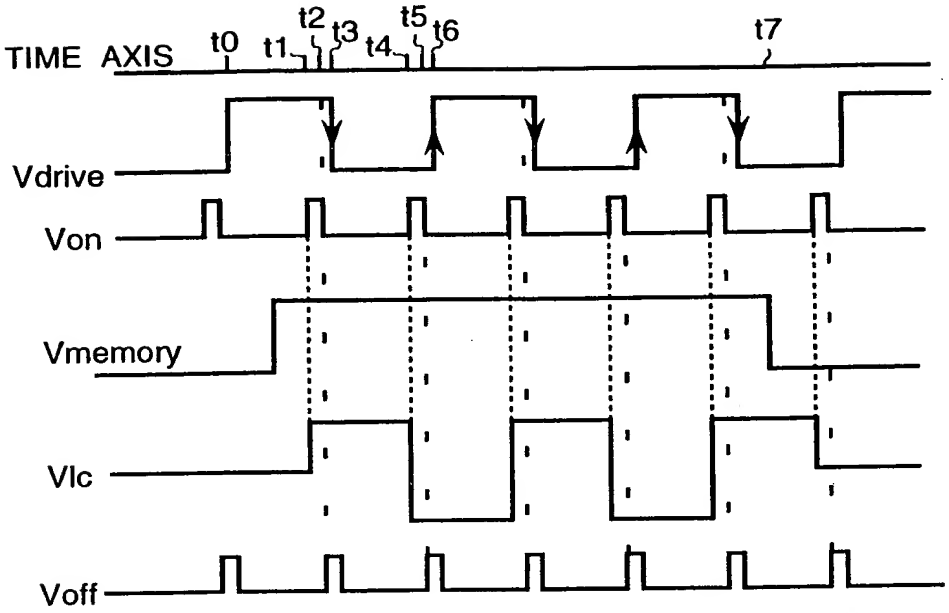

TIME AXIS
t0
t1
t2
t3
t4
t5
t6
t7
Vdrive
Von
Vmemory
Vlc
Voff

FIG.47

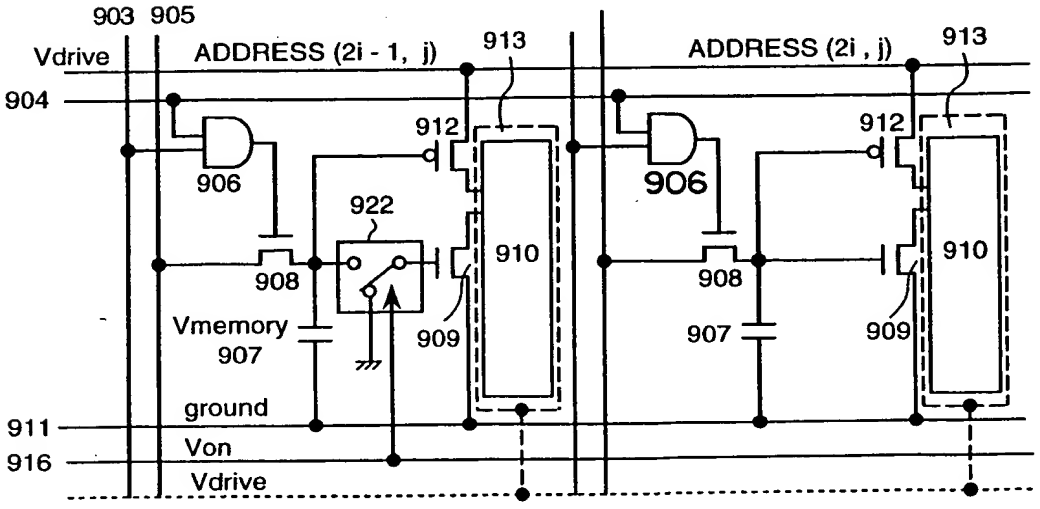

903
905
Vdrive
ADDRESS (2i - 1, j)
913
ADDRESS (2i , j)
913
904
912
912
906
906
922
910
910
908
908
Vmemory
907
909
907
909
ground
911
Von
916
Vdrive

FIG.48

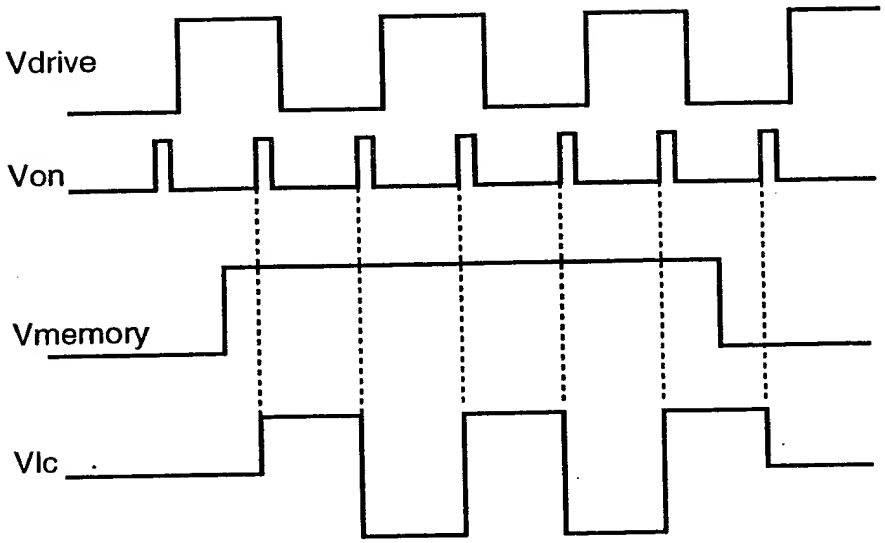

Vdrive
Von
Vmemory
Vlc

FIG.49

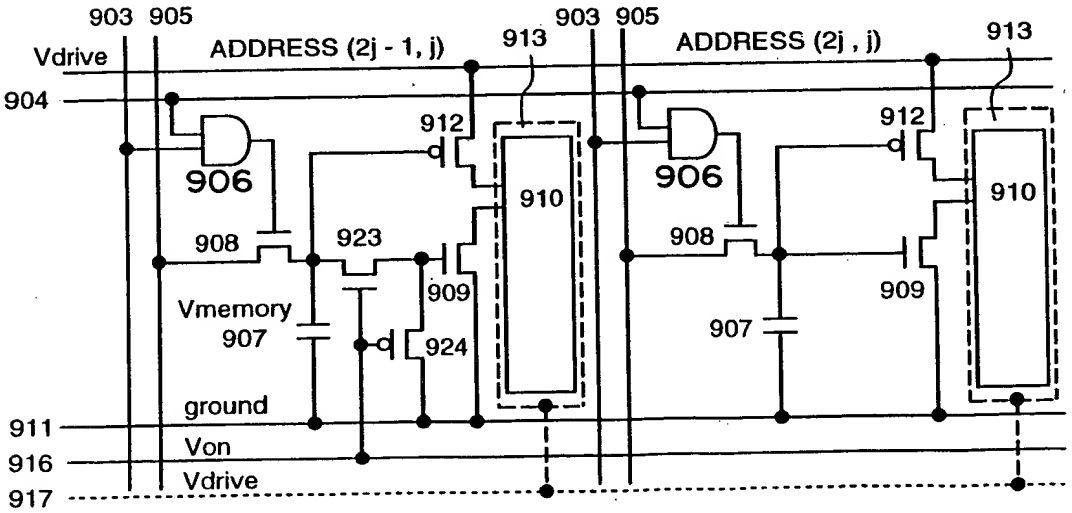

903
905
Vdrive
ADDRESS (2j - 1, j)
913
903
905
ADDRESS (2j , j)
913
904
912
912
906
906
910
910
908
923
908
909
909
Vmemory
907
924
907
ground
911
Von
916
Vdrive
917

FIG.50

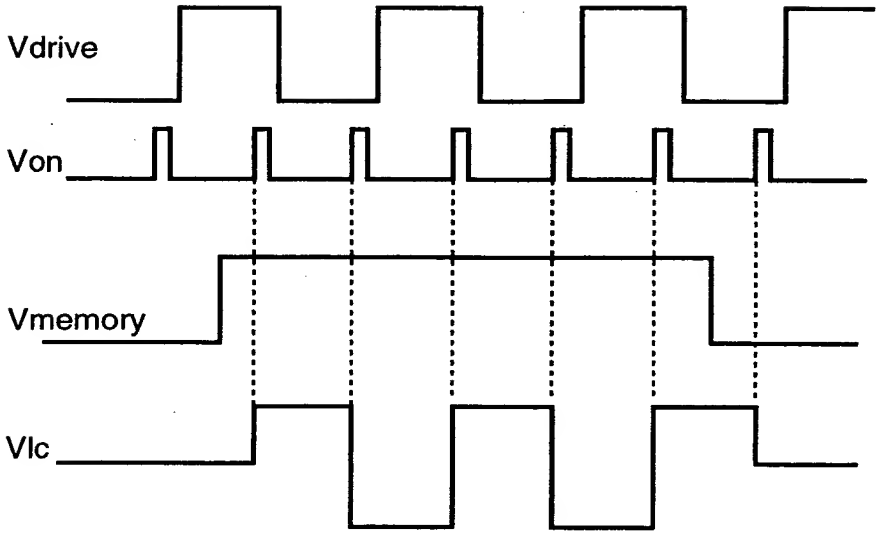
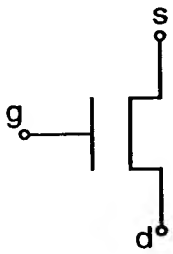
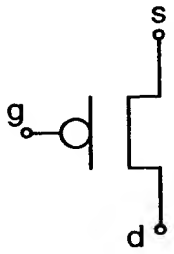


FIG.51A



n - CHANNEL TFT

FIG.51B



p - CHANNEL TFT

FIG.51C